800G OSFP 2xSR4 50m Transceiver

ET8001-2SR4

The ET8001-2SR4 800G is an OSFP 2xVR4 transceiver designed to transmit and receive serial optical data up to 106.25 Gb/s data rate (per channel) by PAM4 modulation over multi-mode fiber. It is a small-form-factor hot-pluggable transceiver module integrated with a high-performance VCSEL laser and high-sensitivity PIN receiver. It is compliant with 800G Ethernet specifications and the OSFP Multi-Source Agreement (MSA).

Product Features

- Up to 106.25Gbps data rate per channel by PAM4 modulation
- 8 duplex-channel transmitters and receivers
- Dual MPO-12 APC optical interfaces
- Selectable Data Rate:106.25Gbps, 53.125Gbps
- Single +3.3 V power supply
- DDM function implemented
- Hot-pluggable OSFP form factor
- Maximum link length of 50 m on OM4 MMF
- Power Dissipation: <16 W
- International Class 1 laser safety certified
- Operating Case Temperature: 25°C ~ +70°C
- Compliant with ROHS6.0

Applications

- 800GBASE-VR8 Ethernet
- Switch and router connections
- Data centers
- Other 800G/2x400G interconnect requirements

Standard

- IEEE 802.3db
- IEEE P802.3ck™/D3.0
- OSFP MSA Rev 5.0
- CMIS Rev 5.1

Ordering Information

Model Name	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Case Temp	Reach	Others	Application
ET8001-2SR4	OSFP	800G	VCSEL	-4.6~4dBm	PD	< -4.4dBm@ 2.4E-4	25~70°C	50m (OM4)	RoHS	800GBase-VR8

Specifications

(Tested under recommended operating conditions, unless otherwise noted)

Transmitter (per Lane)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Signaling Speed per Lane		GBd		53.125±100pm		
Modulation Format				PAM4		
Center Wavelength		nm	844	850	870	
RMS Spectral Width	RMS	nm			0.65	
Average Launch Power per Lane	TXPx	dBm	-4.6		4	
Outer Optical Modulation Amplitude per Lane	OMAouter	dBm	-2.6		3.5	
Transmitter Excursion, each lane	DPx	dB			2.3	
Optical Extinction Ratio	ER	dB	2.5			
Transmitter and Dispersion Penalty Eye Closure for PAM4, each lane	TDECQ	dB			4.4	
Transmitter Transition Time	Tr, Tf	ps			17	
RIN12OMA		dB/Hz			-132	
Encircled Flux	FLX	dBm		>86% at 19um <30%at 4.5um		
Optical Return Loss Tolerance	ORL	dB			14	
Average Launch Power of OFF Transmitter, each lane		dBm			-30	

Receiver (per Lane)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Signaling Speed per Lane		GBd		53.125±100pm		
Modulation Format				PAM4		
Center Wavelength		nm	840		948	
Damage Threshold	DT	dBm	5			
Average Receive Power per Lane	RXPx	dBm	-6.3		4	
Receive Power, each lane (OMA_{outer})		dBm			3.5	
Receiver Reflectance	Rfl	dB			-15	
Receiver Sensitivity (OMA_{outer}),		dBm			-4.4	
Stressed Receiver Sensitivity (OMA_{outer}), each lane	S	dBm			-1.8	BER=2.4E-4

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.3	+3.6

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tca	℃	25	/	70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Bit Rate (Per channel)	BR	Gbps		106.25	
Humidity	Rh	%	5		85
Fiber Bend Radius	Rb	cm	6		

Optical Interface

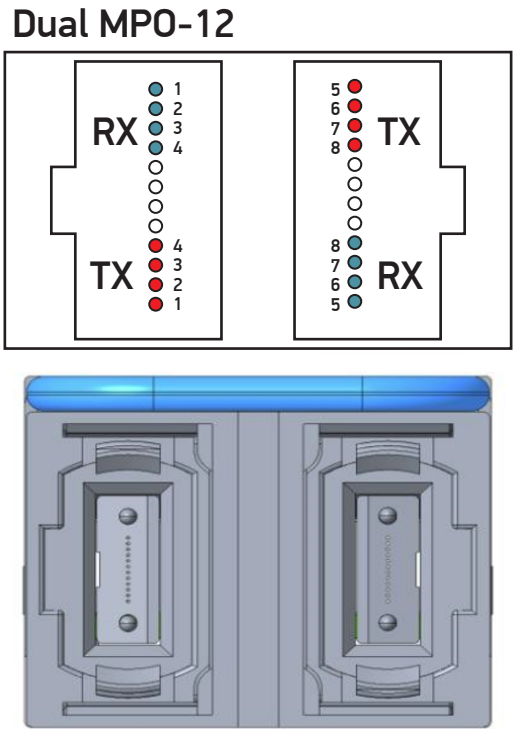
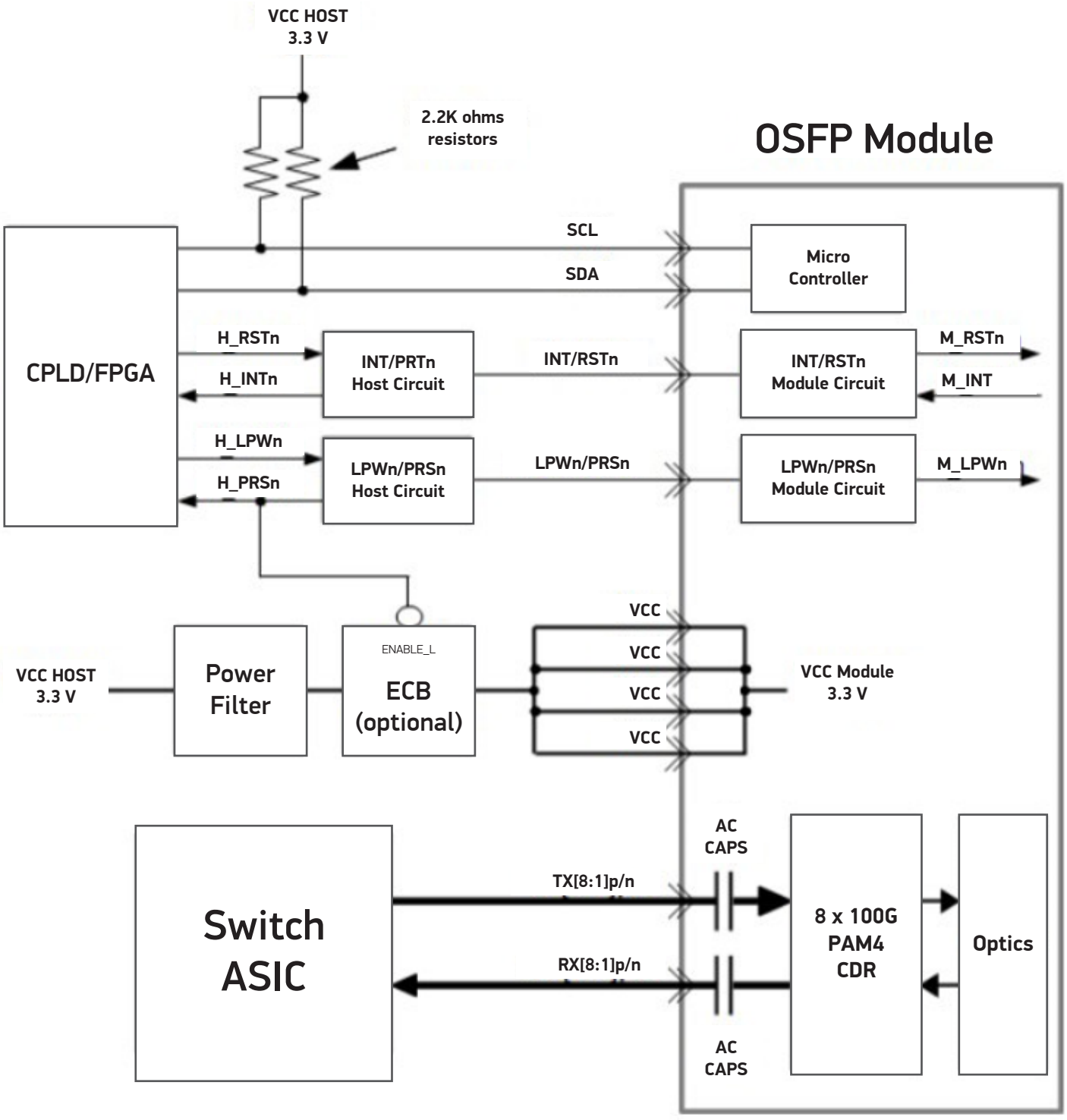


Figure 1. Optical Lane Sequence

Note: Optical interface is 8°dual APC MPO-12. Lane sequence is shown in figure 1.

Principle Diagram



Port Electrical Definition

Parameter	Min.	Typ	Max.	Unit	Notes
Supply Voltage	3.135		3.465	V	
Signaling Rate, each lane	53.125-100ppm	53.125	53.125+100ppm	GBd	

Module Input Characteristics

Parameter	Min.	Typ	Max.	Unit	Notes
Differential Peak-to-Peak Input Voltage Tolerance	750			mV	TP1a
Peak-to-Peak AC Common-Mode Voltage Tolerance Low-Frequency, VCM_{LF}	32			mV	TP1a
Full-Band, VCM_{FB}	80			mV	
Differential-Mode to Common-Mode Return Loss, RLcd	See IEEE Std 802.3ck™-2022 Equation (120G-2)			dB	TP1
Effective Return Loss, ERL	8.5			dB	TP1
Differential Termination Mismatch			10	%	TP1
Module Stressed Input Tolerance	See IEEE Std 802.3ck™-2022 120G.3.4.3			TP1a	
Single-Ended Voltage Tolerance	-0.4		3.3	V	TP1a
DC Common-Mode Voltage Tolerance	-0.35		2.85	V	TP1

Module Output Characteristics

Parameter	Min.	Typ	Max.	Unit	Notes
Peak-to-Peak AC Common-Mode Voltage Low-Frequency, VCM_{LF}			32	mV	TP4
Full-Band, VCM_{FB}			80	mV	
Differential Peak-to-Peak Output Voltage Short Mode			600	mV	TP4
Long Mode			845	mV	
Eye Height	15			mV	TP4
Vertical Eye Closure, VEC			12	dB	TP4
Common-Mode to Differential-Mode Return Loss, RLdc	See IEEE Std 802.3ck™-2022 Equation (120G-1)			dB	TP4
Effective Return Loss, ERL	8.5			dB	TP4
Differential Termination Mismatch			10	%	TP4
Transition Time	8.5			ps	TP4
DC Common-Mode Voltage Tolerance	-0.35		2.85	V	TP4

IIC Communication

Parameter	Min.	Typ	Max.	Unit	Notes
IIC Clock Frequency	100		1000	kHz	
Clock Stretching			500	µs	
Data In Hold Time	0			µs	
Data In Setup Time	0.1			µs	

Pin Description

Pin	Logic	Description
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receive differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3 V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3 V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host.
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module.
VCC	power	3.3 V power for module.
GND	ground	Module ground. Logic and power return path.

Pin List

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	
2	CML-I	Tx2p	Transmitter Data Non-Inverted	
3	CML-I	Tx2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	Tx4p	Transmitter Data Non-Inverted	
6	CML-I	Tx4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	Tx6p	Transmitter Data Non-Inverted	
9	CML-I	Tx6n	Transmitter Data Inverted	
10		GND	Ground	
11	CML-I	Tx8p	Transmitter Data Non-Inverted	
12	CML-I	Tx8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVCMOS-I/O	SCL	2-Wire Serial interface clock	Open-drain with pull-up resistor on host
15		VCC	+3.3 V Power	
16		VCC	+3.3 V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present	See pin description
18		GND	Ground	
19	CML-O	Rx7n	Receiver Data Inverted	
20	CML-O	Rx7p	Receiver Data Non-Inverted	
21		GND	Ground	
22	CML-O	Rx5n	Receiver Data Inverted	
23	CML-O	Rx5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	Rx3n	Receiver Data Inverted	
26	CML-O	Rx3p	Receiver Data Non-Inverted	

Pin List

Pin	Logic	Symbol	Description	Notes
27		GND	Ground	
28	CML-O	Rx1n	Receiver Data Inverted	
29	CML-O	Rx1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	Rx2p	Receiver Data Non-Inverted	
33	CML-O	Rx2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	Rx4p	Receiver Data Non-Inverted	
36	CML-O	Rx4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	Rx6p	Receiver Data Non-Inverted	
39	CML-O	Rx6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	Rx8p	Receiver Data Non-Inverted	
42	CML-O	Rx8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt/Module Reset	See pin description
45		VCC	+3.3 V Power	
46		VCC	+3.3 V Power	
47	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	Open-drain with pull-up resistor on host
48		GND	Ground	
49	CML-I	Tx7n	Transmitter Data Inverted	
50	CML-I	Tx7p	Transmitter Data Non-Inverted	
51		GND	Ground	
52	CML-I	Tx5n	Transmitter Data Inverted	
53	CML-I	Tx5p	Transmitter Data Non-Inverted	
54		GND	Ground	
55	CML-I	Tx3n	Transmitter Data Inverted	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	
57		GND	Ground	
58	CML-I	Tx1n	Transmitter Data Inverted	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	
60		GND	Ground	

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Top Side

60	GND	
59	Tx1p	
58	Tx1n	
57	GND	
56	Tx3p	
55	Tx3n	
54	GND	
53	Tx5p	
52	Tx5n	
51	GND	
50	Tx7p	
49	Tx7n	
48	GND	
47	SDA	
46	VCC	
45	VCC	
44	INT/SRTn	
43	GND	
42	Rx8n	
41	Rx8p	
40	GND	
39	Rx6n	
38	Rx6p	
37	GND	
36	Rx4n	
35	Rx4p	
34	GND	
33	Rx2n	
32	Rx2p	
31	GND	

viewed from top

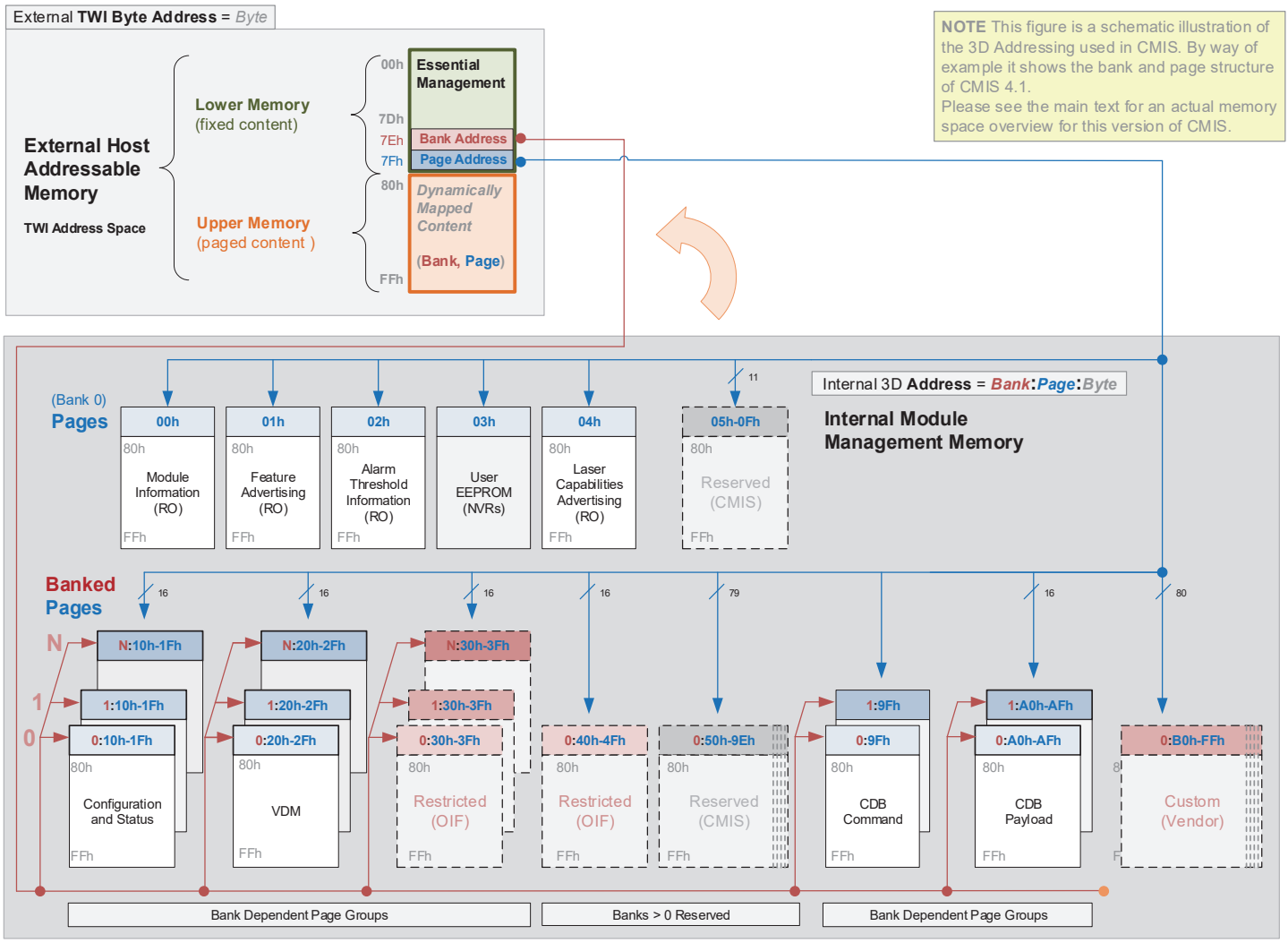
Module Card Edge

Bottom Side

GND	1	
Tx2p	2	
Tx2n	3	
GND	4	
Tx4p	5	
Tx4n	6	
GND	7	
Tx6p	8	
Tx6n	9	
GND	10	
Tx8p	11	
Tx8n	12	
GND	13	
SCL	14	
VCC	15	
VCC	16	
LPWn/PRSn	17	
GND	18	
Rx7n	19	
Rx7p	20	
GND	21	
Rx5n	22	
Rx5p	23	
GND	24	
Rx3n	25	
Rx3p	26	
GND	27	
Rx1n	28	
Rx1p	29	
GND	30	

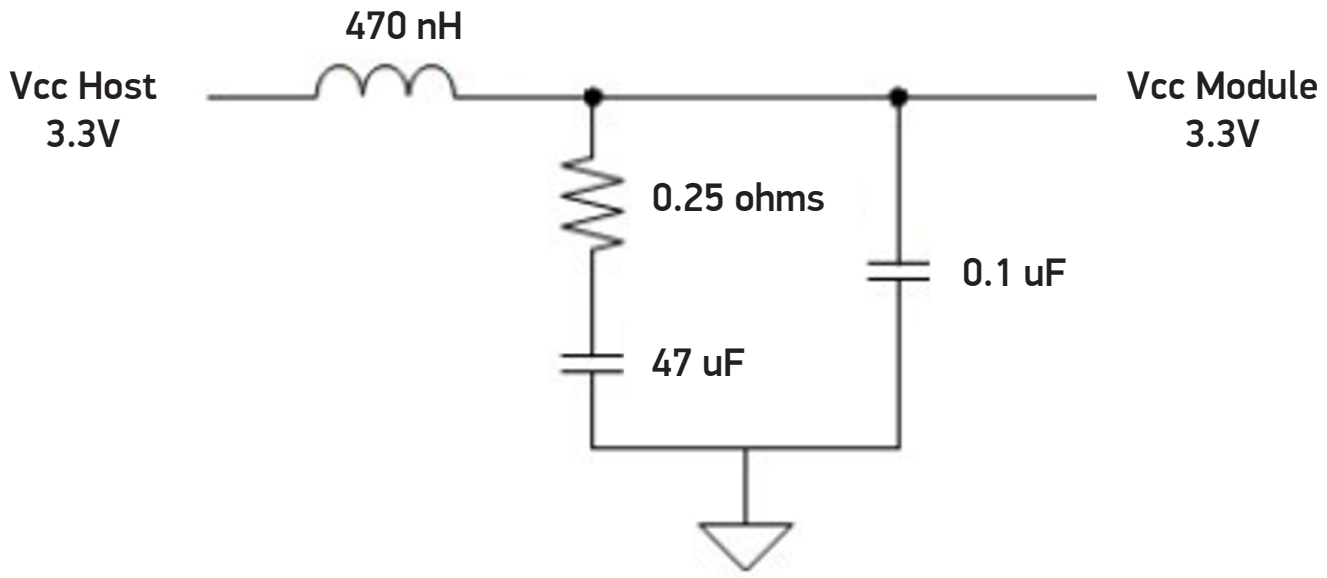
viewed from bottom

Module Memory Map

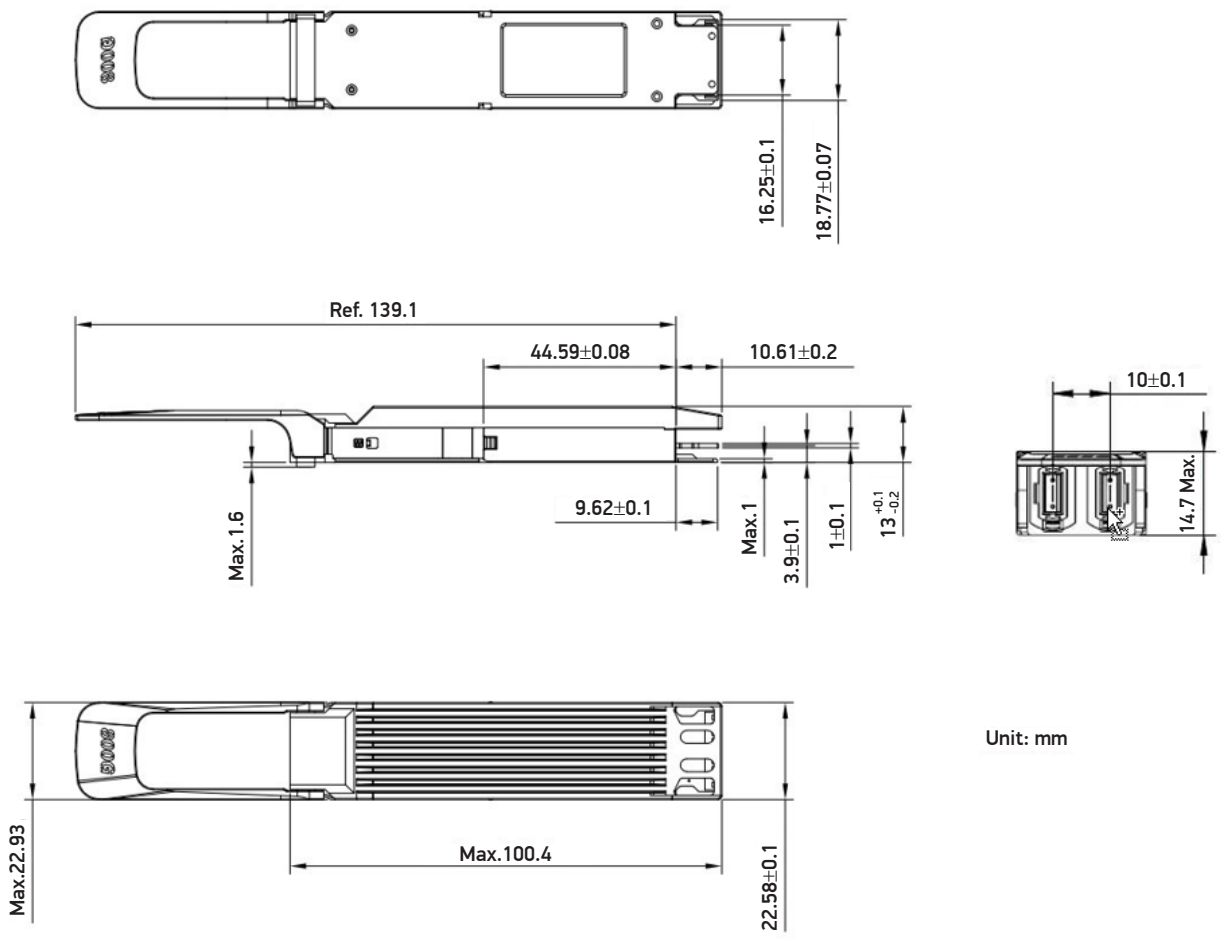


Host Board Power Supply Filtering

This image provides an example implementation for a 3.3 V power filter on the host board. If an alternate circuit is used for power filtering, then the same filter characteristics as this example filter shall be met.



Mechanical Specifications



Unit: mm

Warranty
Please check www.edge-core.com for the warranty terms in your country.

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