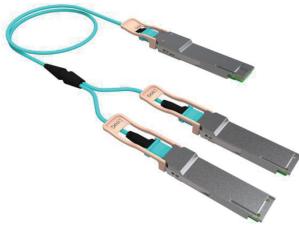


1-30m 400 Gbps to 2 x 200 Gbps Breakout AOC Cable

ET7502-B2A-xxM



The ET7502-B2A-xxM is a 1-30 m active optical breakout cable with one QSFP-DD 400G connector and two QSFP56 200G connectors. The 400G QSFP-DD to 2 x 200G QSFP56 AOC is designed for relatively short connections, offering a low-cost, high-density solution alternative for system providers and customers implementing 400GE/200GE in data centers and cloud networks.

Key Features and Benefits

400G QSFP-DD Features

- Up to 53.125 Gbps data rate per channel by PAM4 modulation
- Supports 400GAUI-8 electrical interface
- Integrated 850nm VCSEL array and PD array
- DDM function implemented
- Hot-pluggable QSFP-DD form factor
- Power Dissipation: <11 W
- Single +3.3V power supply
- Operating Temperature Range: 0°C ~ +70 °C
- Compliant with ROHS10

200G QSFP56 Features

- Up to 53.125 Gbps data rate per channel by PAM4 modulation
- Supports 200GAUI-4 electrical interface
- Integrated 850nm VCSEL array and PD array
- DDM function implemented
- Hot-pluggable QSFP56 form factor
- Power Dissipation: <5.5W
- Single +3.3V power supply
- Operating Temperature Range: 0°C ~ +70 °C
- Compliant with ROHS10

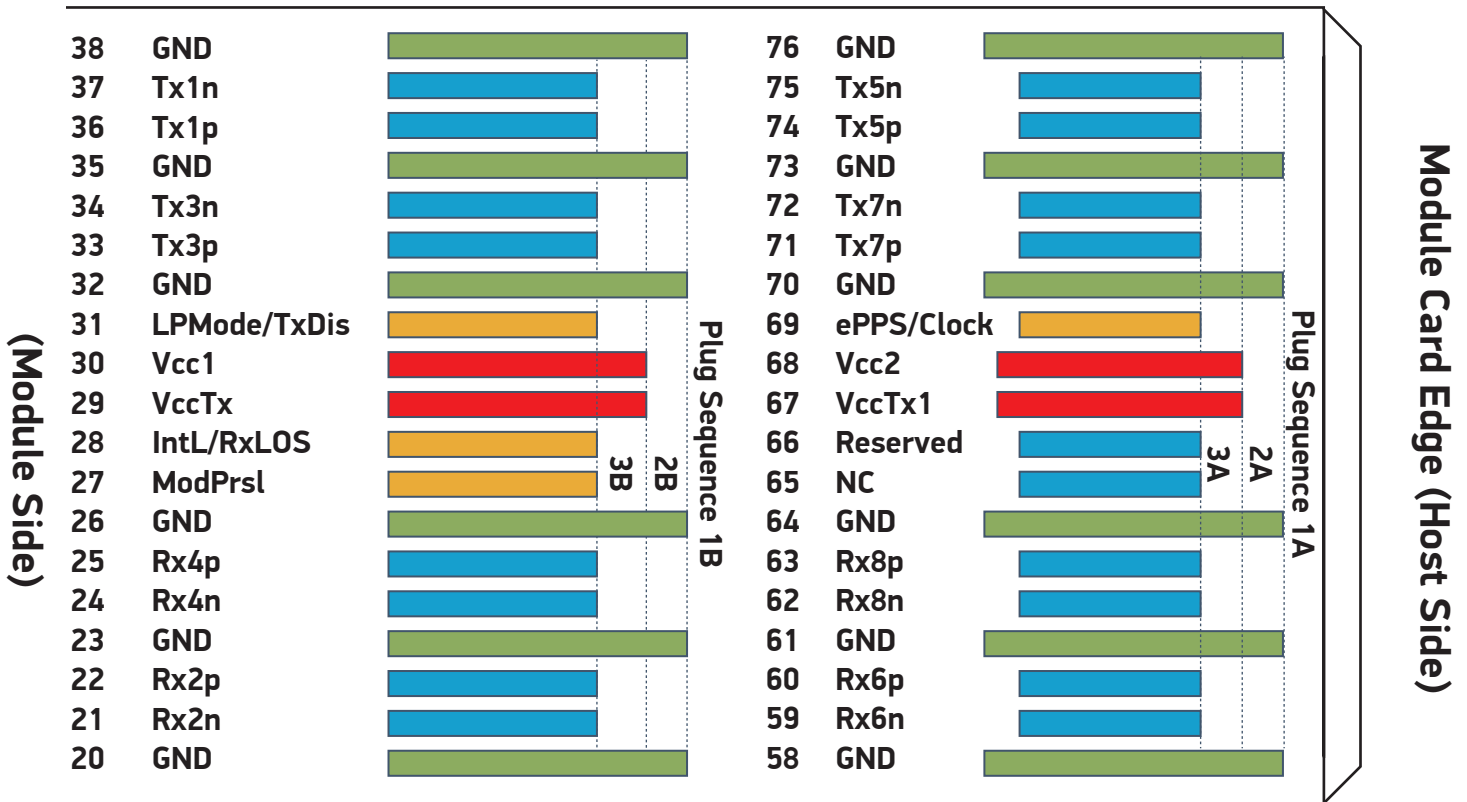
Applications

- Data center cabling infrastructure
- High capacity I/O in storage area networks, network-attached storage, and storage servers
- High-density connections between networking equipment
- Switched fabric I/O such as ultra high-bandwidth switches and routers

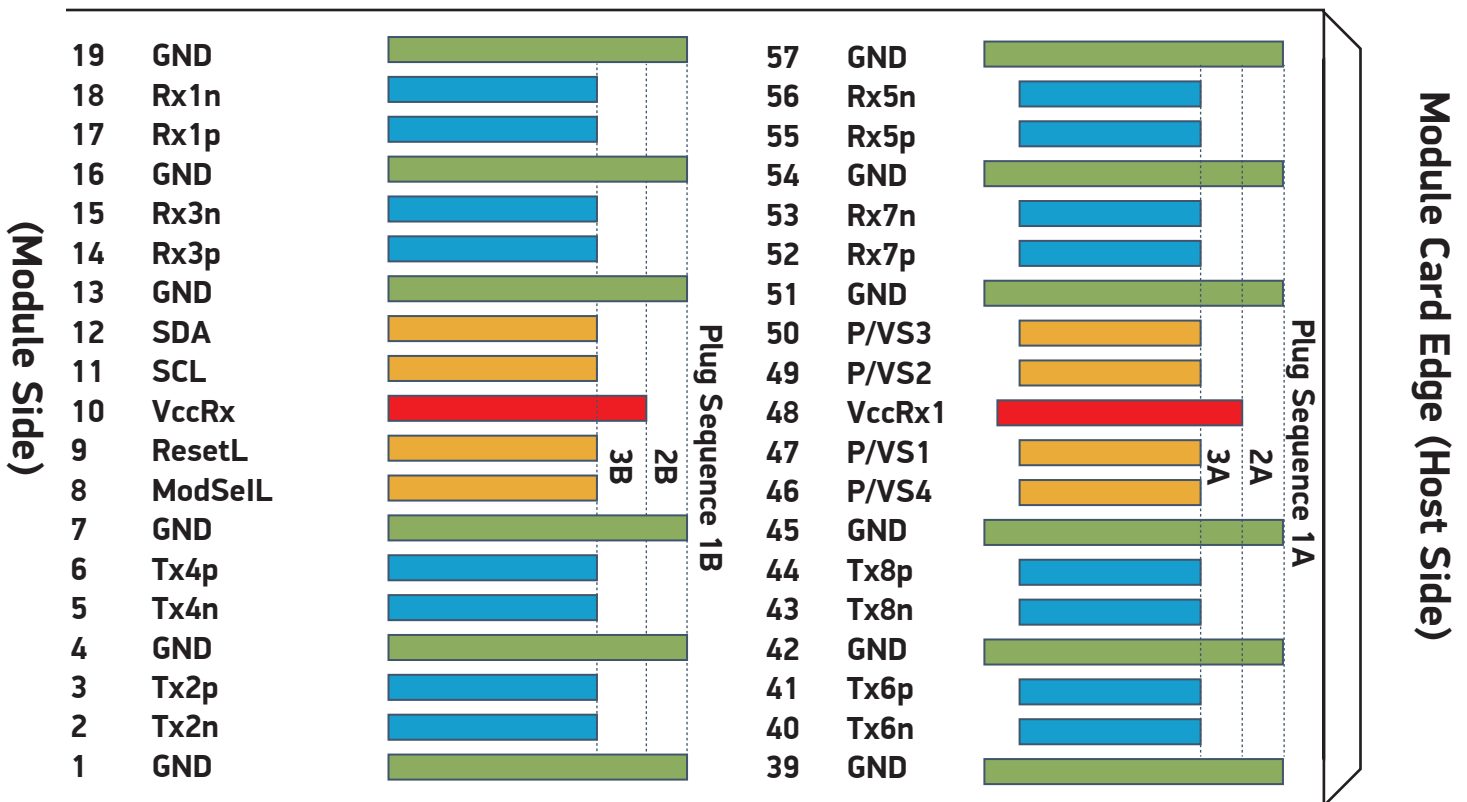
Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	Tst	0	80	°C
Case Operating Temperature	Topc	0	70	°C
Supply Voltage	Vcc3	3.14	3.47	V
Relative Humidity	RH	5	80	%

PCB Viewed From Top



PCB Viewed From Bottom



Electrical Pin-out Details for QSFP-DD

Pad	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTTL-I	ModSelL	Module Select	3B
9	LVTTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVC MOS-I/O	SCL	TWI Serial Interface Clock	3B
12	LVC MOS-I/O	SDA	TWI Serial Interface Data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16		GND	Ground	1B
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTTL-O	ModPrsL	Module Present	3B
28	LVTTTL-O	IntL/RxLOS	Interrupt/Optional RxLOS	3B
29		VccTx	+3.3 V Power Supply Transmitter	2B
30		Vcc1	+3.3 V Power Supply	2B
31	LVTTTL-I	LPMoDe/TxDis	Low Power Mode/Optional TX Disable	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B

Electrical Pin-out Details for QSFP-DD

Pad	Logic	Symbol	Description	Plug Sequence
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46	LVC MOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A
47	LVC MOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49	LVC MOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A
50	LVC MOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For Future Use	3A
67		VccTx1	3.3 V Power Supply	2A
68		Vcc2	3.3 V Power Supply	2A
69	LVC MOS-I	ePPS/Clock	1PPS PTP Clock or Reference Clock Input	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

Pin Description

38	GND	
37	TX1n	
36	TX1p	
35	GND	
34	TX3n	
33	TX3p	
32	GND	
31	LPMoDe/TxDis	
30	Vcc1	
29	VccTx	
28	IntL/RxLOSL	
27	ModPrsL	
26	GND	
25	RX4p	
24	RX4n	
23	GND	
22	RX2p	
21	Rx2n	
20	GND	

**Top Side
Viewed From Top**

Module Card Edge

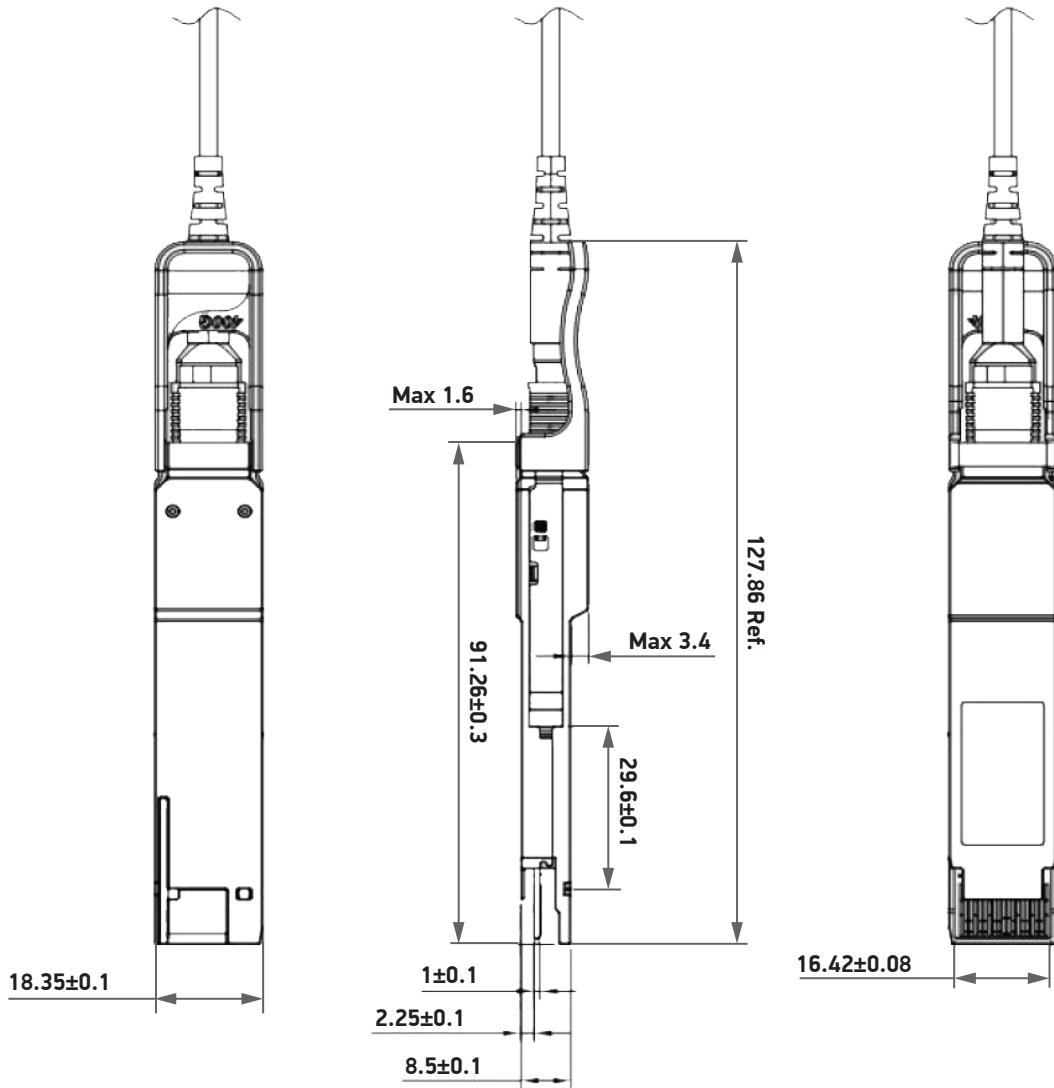
	GND	1
	TX2n	2
	TX2p	3
	GND	4
	TX4n	5
	TX4p	6
	GND	7
	ModSelL	8
	ResetL	9
	VccRx	10
	SCL	11
	SDA	12
	GND	13
	RX3p	14
	RX3n	15
	GND	16
	RX1p	17
	RX1n	18
	GND	19

**Bottom Side
Viewed From Bottom**

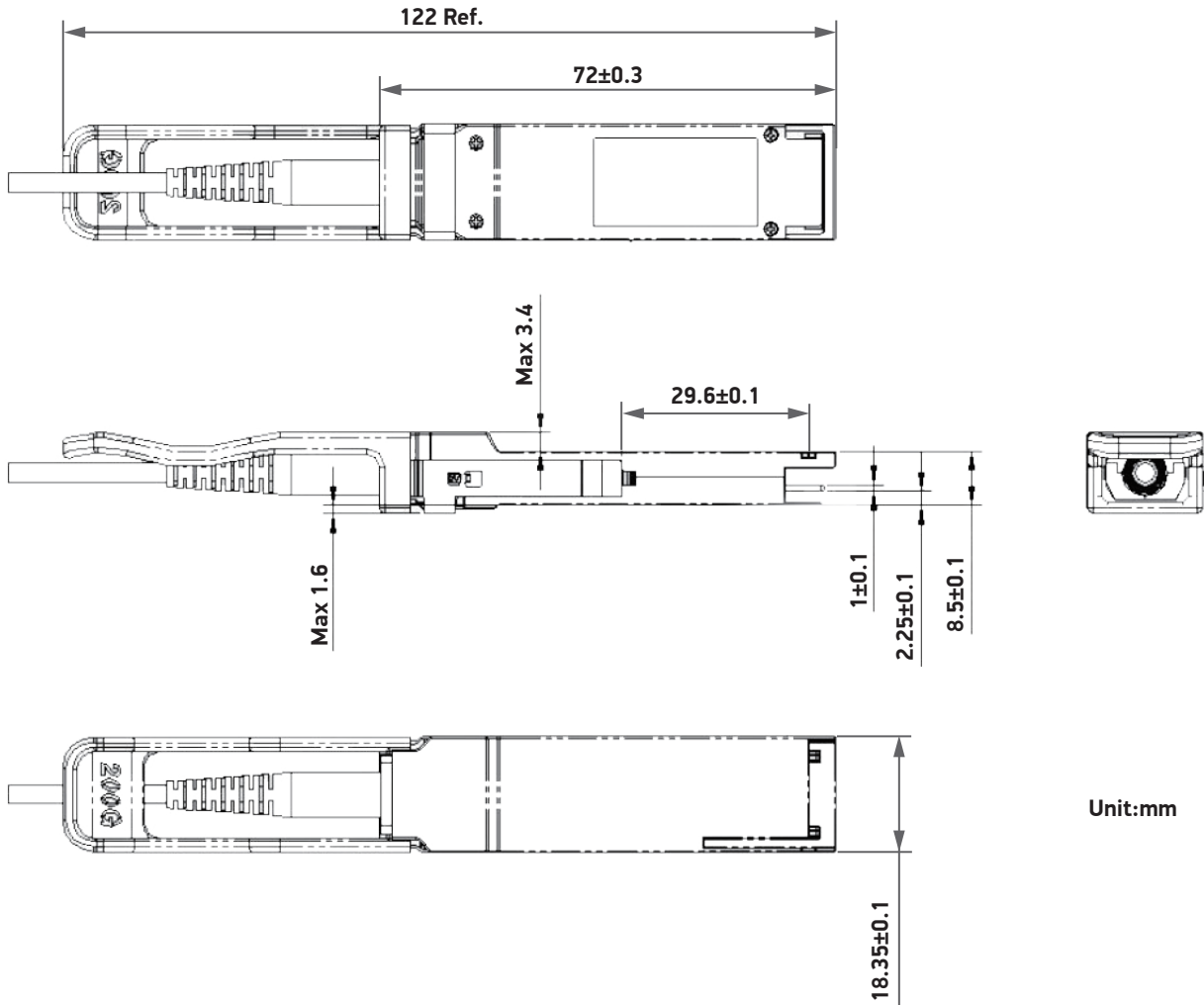
Electrical Pin-out Details for QSFP56

Pad	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTTL-I	ModSelL	Module Select	3
9	LVTTTL-I	ResetL	Module Reset	3
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-wire Serial Interface Clock	3
12	LVC MOS-I/O	SDA	2-wire Serial Interface Data	3
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3
18	CML-O	Rx1n	Receiver Inverted Data Output	3
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3
26		GND	Ground	1
27	LVTTTL-O	ModPrsL	Module Present	3
28	LVTTTL-O	IntL	Interrupt	3
29		VccTx	+3.3 V Power Supply Transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTTL-I	LPMODE	Low Power Mode	3
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3
37	CML-I	Tx1n	Transmitter Inverted Data Input	3
38		GND	Ground	1

Mechanical Drawing (QSFP-DD)



Mechanical Drawing (QSFP56)



Unit:mm

Ordering Information

Package	Data Rate	Length	Region
QSFP-DD/QSFP56	400G/200G	xx=1-30	All

Warranty

Please check www.edge-core.com for the warranty terms in your country.

For More Information

To find out more about Edgecore Networks Corporation products and solutions, visit www.edge-core.com.

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