

# 400 Gbps QSFP-DD ZR Coherent Transceiver

## ECPO-QDDZR400G



The ECPO-QDDZR400G is a 400 Gbps tunable dense wavelength division multiplexing (DWDM) DP-16QAM coherent transceiver. The QSFP-DD form factor device is hot pluggable and includes digital diagnostics monitoring (DDM) and control functions. This module enables interoperable and cost-effective solutions (OIF Type-1) for WDM transmission links up to 120 km.

This transceiver employs coherent optic techniques and its key components include a nano-integrable tunable laser assembly (ITLA), a 7-nm coherent digital signal processing (DSP) chip, and a silicon-photonics-based coherent transmitter and receiver optical assembly (COSA).

The transceiver supports one 400GAUI-8 (PAM4) Ethernet interface on the client side, which is fully compatible with an IEEE 802.3 400GAUI-8 C2M to OIF 400GE-ZR client/host system. The transceiver uses a single-carrier 60 GBaud coherent DP-16QAM modulation format on the line side. Concatenated FEC (C-FEC) enables a post-FEC error floor of  $<1e-15$  with a pre-FEC BER threshold of  $1.25e-2$ .

The transceiver can be conveniently plugged into the host system through its pull tab. The transceiver operates from a single +3.3 V power supply over an operating case temperature range of 0°C to +70°C. The housing is made of metal for EMI immunity.

The common management interface is implemented as a two-wire interface (I2C bus) for serial ID, digital diagnostics, and module control functions. An enhanced digital diagnostics monitoring interface allows real-time access to the device for monitoring transmitted optical power, received optical power, SNR, BER, and laser wavelength, etc.

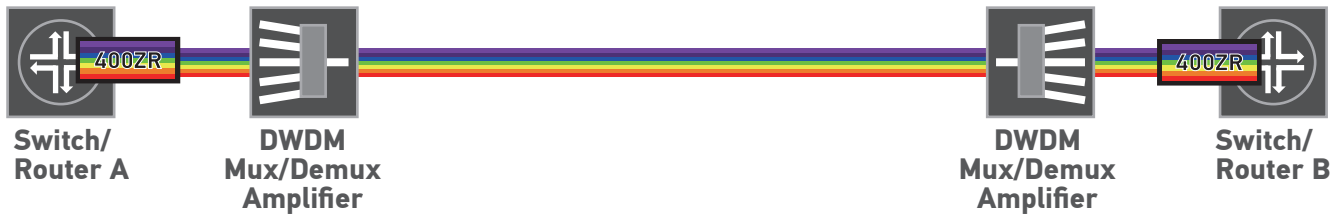
### Product Features

- 400 Gbps dense wavelength division multiplexing (DWDM) over 75/100-GHz spacing in full C-band
- Coherent optical Tx and Rx in the MSA QSFP-DD Type 2 form factor
- DP-16QAM modulation
- Supports OIF C-FEC
- Power consumption max 19 W (typical  $<18$  W)
- 0°C to +70°C operating case temperature
- Compliant with OIF-400ZR implementation agreement and QSFP-DD CMIS revision 5.0
- Duplex LC receptacles
- RoHS Compliant

### Ordering Information

Edgecore Model Name	Case Operating Temperature	Wavelength (nm)	ITU Frequency (THz)	Type
ECPO-QDDZR400G	0°C to +70°C	Tunable	Full C-band 75/100GHz Grids	400G QSFP-DD ZR

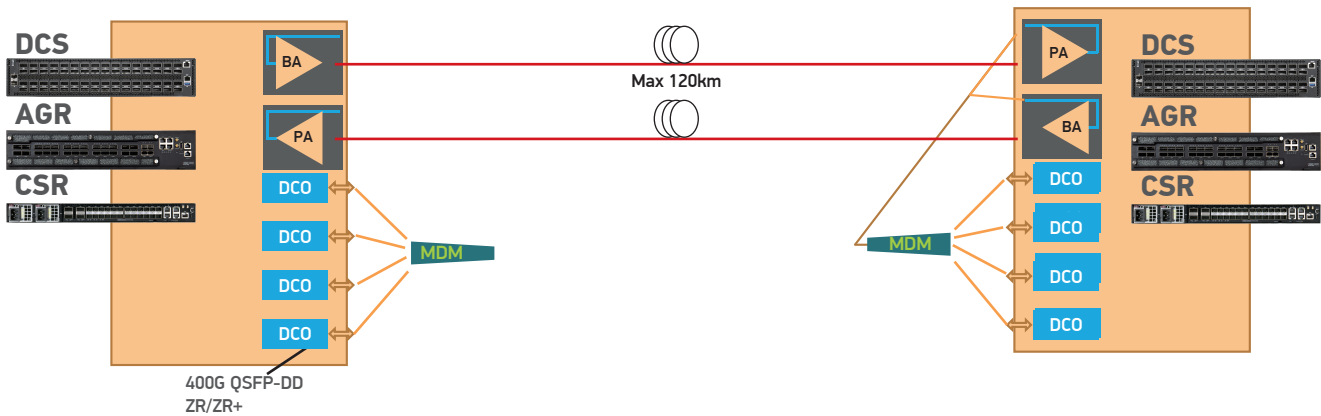
According to the OIF-400ZR implementation agreement, the ECPO-QDDZR400G supports three use cases for 120 km or less, amplified, point-to-point, DWDM noise limited links. Two of the use cases require separate transponder systems. The other use case, where the 400G ZR transceiver is plugged into the switch/router, enables the IPoDWDM applications for DWDM IP signal channels from the switch/router to be directly sent onto the link with EDFA amplifiers and optional DWDM Mux/Demux.



Router/Switch with 400GE-ZR DWDM Interfaces (from OIF-400ZR-01.0 Specs)

Although EDFA amplifiers and DWDM Mux/Demux are widely available as additional optical transport systems to deploy alongside switches/routers, Edgecore has developed a pluggable EDFA in a QSFP28 form factor to support both Booster-Amp (BA) and Pre-Amp (PA) configurations.

A compact cable-style DWDM Mux/Demux (MDM) is also available to completely remove the need of a separate optical transport system, as shown below:



For detailed information on the 400GE-ZR support for Edgecore’s DCS, AGR and CSR switch/router platforms, please refer to our website <https://www.edge-core.com>.

Product information for the pluggable EDFA and compact MDM is published under <https://www.edge-core.com/productsList.php?cls=4&cls2=28&cls3=668>.

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature Range	$T_{ST}$	- 40	+ 85	°C
Case Operating Temperature	$T_{OP}$	0	+ 70	°C
Operating Relative Humidity <sup>1</sup>	RH	5	85	%
Supply Voltage Range	$V_{CC}$	- 0.3	+ 3.6	V

<sup>1</sup>Non-condensing

## Transmitter Performance Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit
Data Rate	B	-	59.84375	-	GBd
Encoding Type	-	-	DP-16QAM	-	-
Grid Spacing	-	-	25	-	GHz
Center Frequency (OIF Type 1)	$f_c$	191.3	-	196.1	THz
Frequency Precision	-	-	-	1.8	GHz
Frequency Set Resolution	-	100	-	-	MHz
Power Stability	-	-0.5	-	0.5	dB
Power Setting Accuracy	-	-1.0	-	1.0	dB
Output Power (OIF Type 1)	$P_o$	-10	-	-	dBm
Output Out-of-Band OSNR	$OSNR_{out-of-band}$	23	-	-	dB/0.1nm
Output In-Band OSNR	$OSNR_{in-band}$	34	-	-	dB/0.1nm
Return Loss	IL	20	-	-	dB
Disable Launch Output Power	$P_{off}$	-	-	-20	dBm

## Receiver Performance Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit
Data Rate	B	-	59.84375	-	GBd
Encoding Type	-	-	DP-16QAM	-	-
Dispersion Compensation (OSNR Penalty <0.5 dB)	-	-	+/- 2400	-	ps/nm
PMD Tolerance Range (OSNR Penalty <0.5 dB)	-	10	-	-	ps
OSNR Sensitivity (OIF Type 1)	-	-	24.5	26	dB @ 0.1 nm
Power Sensitivity @ OSNR Threshold (OIF Type 1)	-	-	-	-12.0	dBm
Optical Return Loss	IL	20	-	-	dB
Damage Threshold	-	15	-	-	dBm

### Low Speed Pin Electrical Specifications

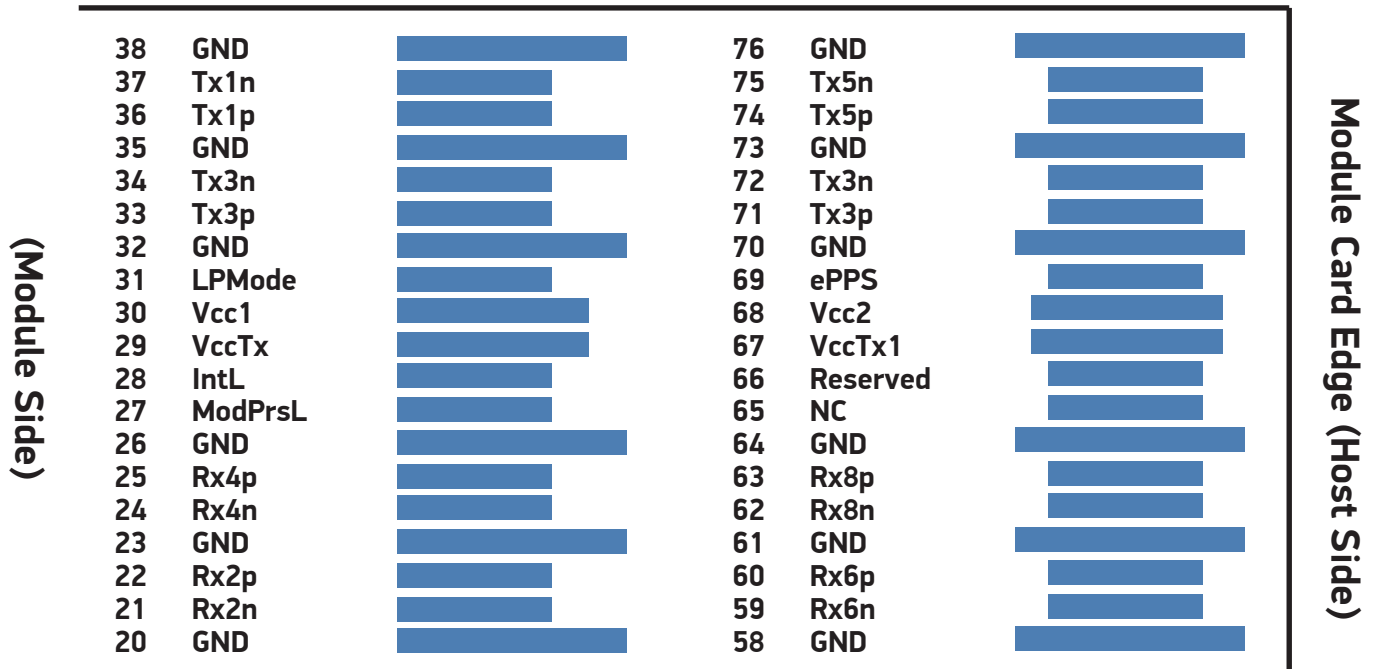
Parameter	Symbol	Min.	Max	Unit	Condition
SCL and SDA	$V_{OL}$	0	0.4	V	$I_{OL}$ (max)=3mA for fast mode, 20mA for fast mode plus.
SCL and SDA	$V_{IL}$	-0.3	$V_{CC} \cdot 0.3$	V	
	$V_{IH}$	$V_{CC} \cdot 0.7$	$V_{CC} + 0.5$	V	
Capacitance for SCL and SDA I/O Signal	$C_i$		14	pF	
Total Bus Capacitive Load for SCL and SDA	$C_b$		100	pF	For 400kHz clock rate use 3.0 kOhms pullup resistor, max.
			200	pF	For 400kHz clock rate use 3.0 kOhms pullup resistor, max.
InitMode, ResetL and ModSelL	$V_{IL}$	-0.3	0.8	V	
	$V_{IH}$	2	$V_{CC} + 0.3$	V	
	$ I_{in} $		360	uA	$0V < V_{in} < V_{CC}$
IntL	$V_{OL}$	0	0.4	V	$I_{OL} = 2.0mA$
	$V_{OH}$	$V_{CC} - 0.5$	$V_{CC} + 0.3$		10 kOhms pull-up to Host Vcc
ModPrsL	$V_{OL}$	0	0.4	V	$I_{OL} = 2.0mA$
	$V_{OH}$				ModPrsL can be implemented as a short-circuit to GND on the module

### Electrical Power Supply Characteristics

Parameter	Symbol	Min	Typical	Max	Units
Power Supply Voltage	Vcc	3.14	3.30	3.47	V
Power Consumption	$P_w$	-	<18	19	W

Electrical Pad Layout

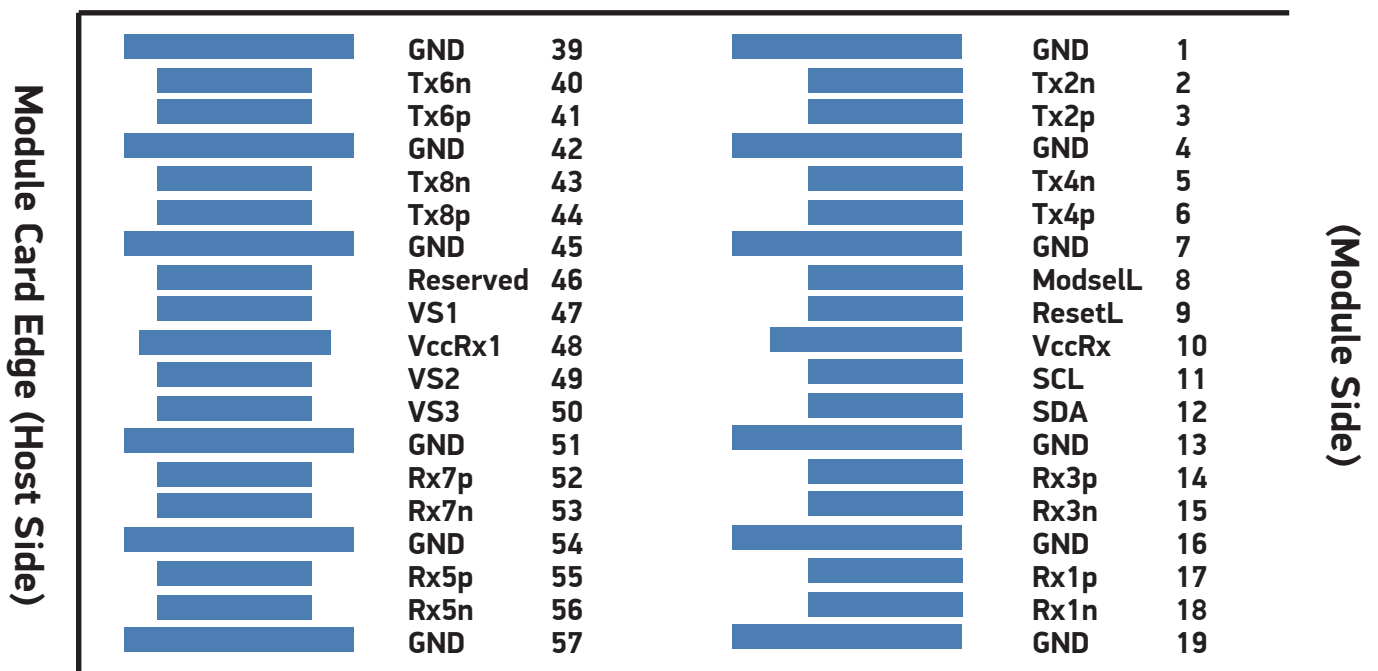
Top side viewed from top



Legacy QSFP28 Pads

Additional QSFP-DD Pads

Bottom side viewed from bottom



Additional QSFP-DD Pads

Legacy QSFP28 Pads

## Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence <sup>4</sup>
1		GND	Ground <sup>1</sup>	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground <sup>1</sup>	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground <sup>1</sup>	1B
8	LVTTL-I	ModSelL	Module Select.	3B
9	LVTTL-I	ResetL	Module Reset.	3B
10		VccRx	+3.3 V Power Supply Receiver <sup>2</sup>	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground <sup>1</sup>	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16		GND	Ground <sup>1</sup>	1B
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground <sup>1</sup>	1B
20		GND	Ground <sup>1</sup>	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground <sup>1</sup>	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground <sup>1</sup>	1B
27	LVTTL-O	ModPrsL	Module Present.	3B
28	LVTTL-O	IntL	Interrupt.	3B
29		VccTx	+3.3 V Power supply transmitter <sup>2</sup>	2B
30		Vcc1	+3.3 V Power supply <sup>2</sup>	2B
31	LVTTL-I	LPMODE	Low Power Mode	3B
32		GND	Ground <sup>1</sup>	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground <sup>1</sup>	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground <sup>1</sup>	1B

## Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence <sup>4</sup>
39		GND	Ground <sup>1</sup>	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground <sup>1</sup>	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground <sup>1</sup>	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific <sup>3</sup>	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific <sup>2</sup>	3A
50		VS3	Module Vendor Specific <sup>3</sup>	3A
51		GND	Ground <sup>1</sup>	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground <sup>1</sup>	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground <sup>1</sup>	1A
58		GND	Ground <sup>1</sup>	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground <sup>1</sup>	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground <sup>1</sup>	1A
65		NC	No Connect	3A
66		Reserved	For future use	3A
67		VccTx1	3.3 V Power Supply	2A
68		Vcc2	3.3 V Power Supply	2A
69	LVTTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A
70		GND	Ground <sup>1</sup>	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground <sup>1</sup>	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground <sup>1</sup>	1A

Note 1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3. All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see page 4 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

**Warranty**

Please check [www.edge-core.com](http://www.edge-core.com) for the warranty terms in your country.

**For More Information**

To find out more about Edgecore Networks Corporation products and solutions, visit [www.edge-core.com](http://www.edge-core.com).

**About Edgecore Networks Corporation**

Edgecore Networks Corporation is in the business of providing innovative network solutions. In the service provider network, in the data center or in the cloud, Edgecore Networks Corporation delivers the software and systems that transform the way the world connects. Edgecore Networks Corporation serves customers and partners worldwide. Additional information can be found at [www.edge-core.com](http://www.edge-core.com).

Edgecore Networks Corporation is a subsidiary of Accton Technology Corporation, the leading network ODM company. The Edgecore data center switches are developed and manufactured by Accton.

To purchase Edgecore Networks solutions, please contact your Edgecore Networks Corporation representatives at +886 3 563 8888 (HQ) or +1 (949)-336-6801 or authorized resellers.

© Copyright 2023 Edgecore Networks Corporation. The information contained herein is subject to change without notice. This document is for informational purposes only and does not set forth any warranty, expressed or implied, concerning any equipment, equipment feature, or service offered by Edgecore Networks Corporation. Edgecore Networks Corporation shall not be liable for technical or editorial errors or omissions contained herein.