800G QSFP-DD SR8 50m Transceiver

ET8002-SR8

The ET8002-SR8 is an 800G QSFP-DD SR8 transceiver designed to transmit and receive serial optical data up to 106.25 Gbps data rate (per channel) by PAM4 modulation over multimode fiber. It is a small-form-factor hot-pluggable transceiver module integrated with a high-performance VCSEL laser and high-sensitivity PIN receiver. It is compliant with 800G Ethernet and the QSFP-DD MSA.

Product Features

- Up to 106.25 Gbps data rate per channel by PAM4 modulation on media side
- Up to 106.25 Gbps data rate per channel by PAM4 modulation on host side
- MPO-16 APC optical interface
- Single +3.3V power supply
- DDM function implemented
- Hot-pluggable QSFP-DD form factor
- Maximum link length of 50M on OM4 MMF
- Power dissipation: <16 W
- International Class 1 laser safety certified
- Operating temperature range: 25°C ~ +70°C
- Compliant with ROHS2.0

Applications

- 800GBASE Ethernet
- Switch and router connections
- Data centers
- Other 800G interconnect requirements.

Standards

- IEEE 802.3df
- IEEE P802.3ck™/D3.0
- QSFP-DD HW Rev 6.2
- CMIS Rev 4.0 or later version

Ordering Information

Model Name	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Case Temp	Reach	Others	Application
ET8002-SR8	QSFP-DD	800G	VCSEL	-4.6~4dBm	PD	< -4.4dBm@2.4E-4	25~70°C	50m (OM4)	RoHS	800GBase-SR8

Specifications

(Tested under recommended operating conditions, unless otherwise noted)

Transmitter (per Lane)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Signaling Speed per Lane		GBd		53.125±50ppm		
Modulation Format				PAM4		
Center Wavelength		nm	844	850	870	
RMS Spectral Width	RMS	nm			0.65	
Average Launch Power per Lane	TXPx	dBm	-4.6		4	
Outer Optical Modulation Amplitude per Lane	OMAouter	dBm	-2.6		3.5	
Transmitter Excursion, each lane	DPx	dB			2.3	
Optical Extinction Ratio	ER	dB	2.5			
Transmitter and Dispersion Penalty Eye Closure for PAM4, each lane	TDECQ	dB			4.4	
Transmitter Transition Time	Tr, Tf	ps			17	
RIN12OMA		dB/Hz			-132	
Encircled Flux	FLX	dBm		>86% at 19um <30%at 4.5um		
Optical Return Loss Tolerance	ORL	dB			14	
Average Launch Power of OFF Transmitter, each lane		dBm			-30	

Receiver (per Lane)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Signaling Speed per Lane		GBd		53.125±50ppm		
Modulation Format				PAM4		
Center Wavelength		nm	840		948	
Damage Threshold	DT	dBm	5			
Average Receive Power per Lane	RXPx	dBm	-6.3		4	
Receive Power, each lane (OMAouter)		dBm			3.5	
Receiver Reflectance	Rfl	dB			-15	
Receiver Sensitivity (OMAouter),		dBm			-4.4	
Stressed Receiver Sensitivity (OMAouter), each lane	S	dBm			-1.8	BER=2.4E-4

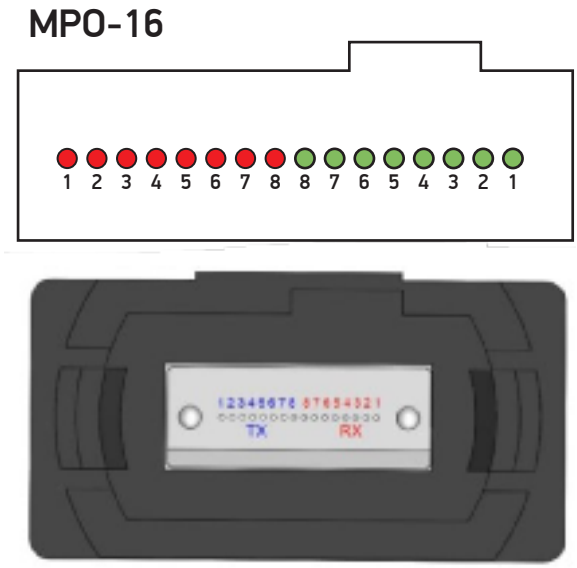
Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.3	+3.6

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tca	℃	25	/	70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Bit Rate (per channel)	BR	Gbps		106.25	
Humidity	Rh	%	5		85
Fiber Bend Radius	Rb	cm	6		

Optical Interface



Note: Optical interface is 8°dual APC MPO-16. Lane sequence is shown in the figure above.

Electrical Pin Description

Pin	Name	Function/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL/RxLOS	Interrupt/Optional RxLOS	
29	VccTx	3.3 V Power Supply Transmitter	2
30	Vcc1	3.3 V Power Supply	2
31	LPMode/TxDis	Low Power Mode/Optional TX Disable	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	

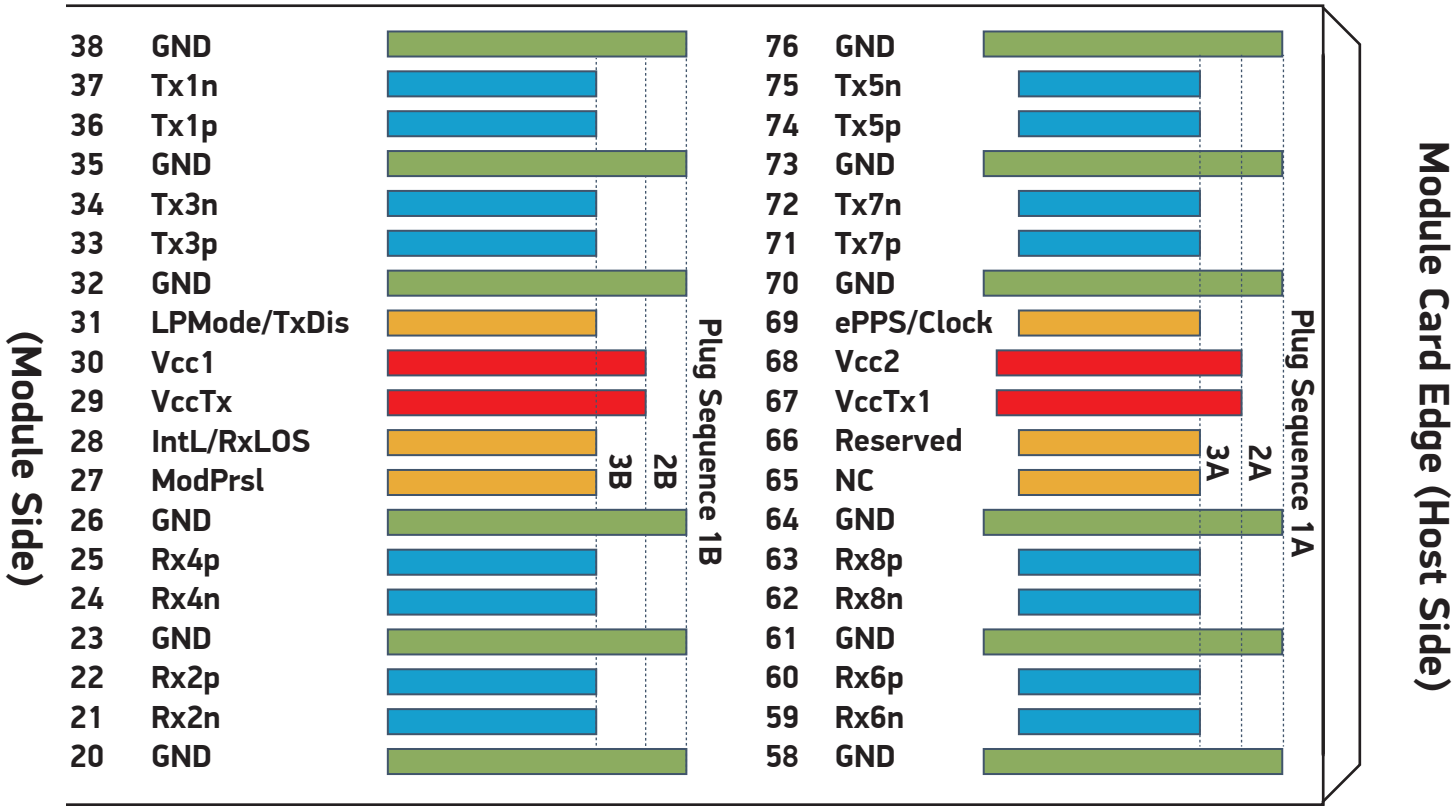
Electrical Pin Description

Pin	Name	Function/Description	Notes
44	Tx8p	Transmitter Non-Inverted Data Input	
45	GND	Ground	1
46	P/VS4	Programmable/Module Vendor Specific 4	4
47	P/VS1	Programmable/Module Vendor Specific 1	4
48	VccRx1	3.3V Power Supply	2
49	P/VS2	Programmable/Module Vendor Specific 2	4
50	P/VS3	Programmable/Module Vendor Specific 3	4
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3 V Power Supply	2
68	Vcc2	3.3 V Power Supply	2
69	ePPS/Clock	1PPS PTP Clock or Reference Clock Input	5
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	1

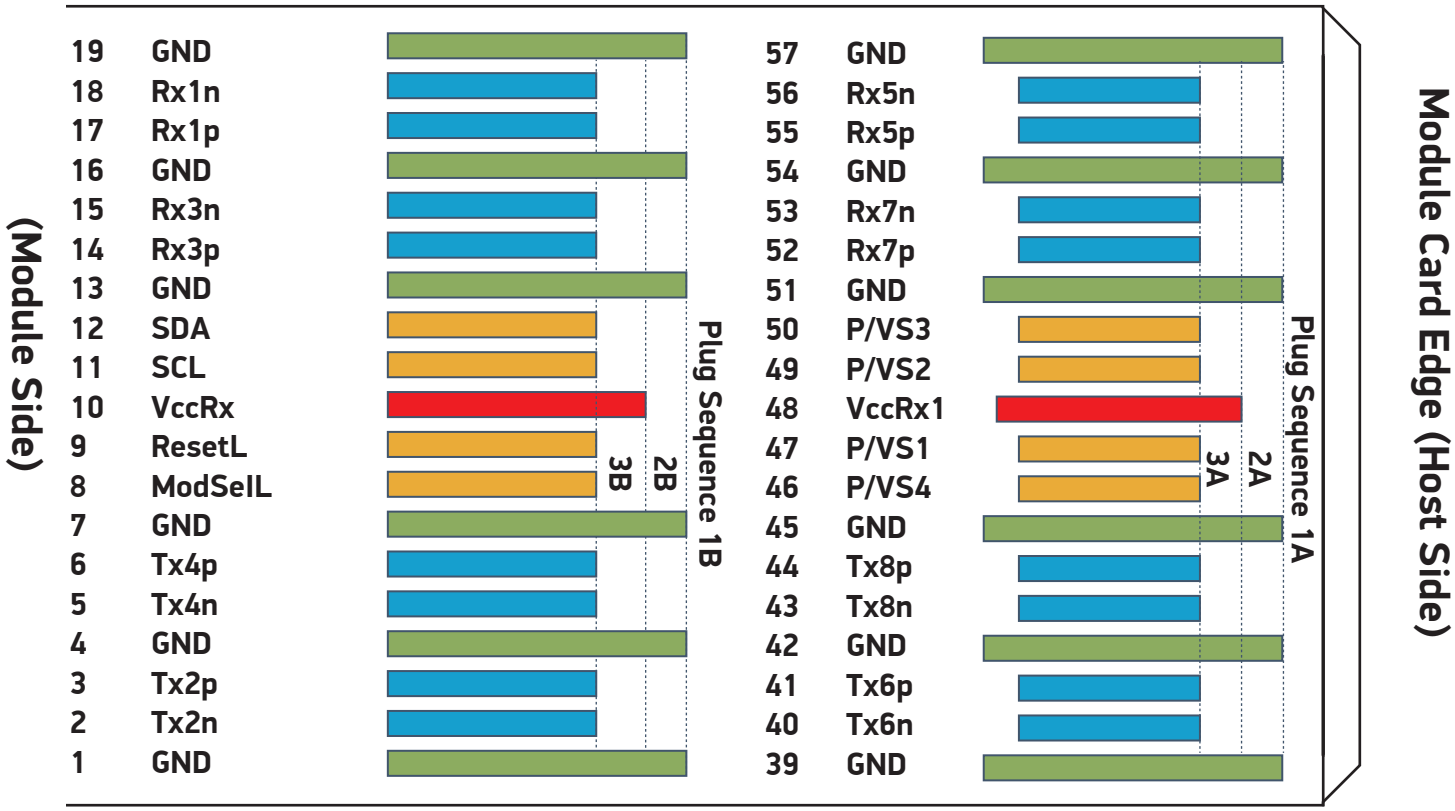
Note:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a steady state current of 500mA.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500mA.
3. Reserved pad recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 kΩ to ground on the host.
4. Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.
5. For host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module.

PCB Viewed From Top

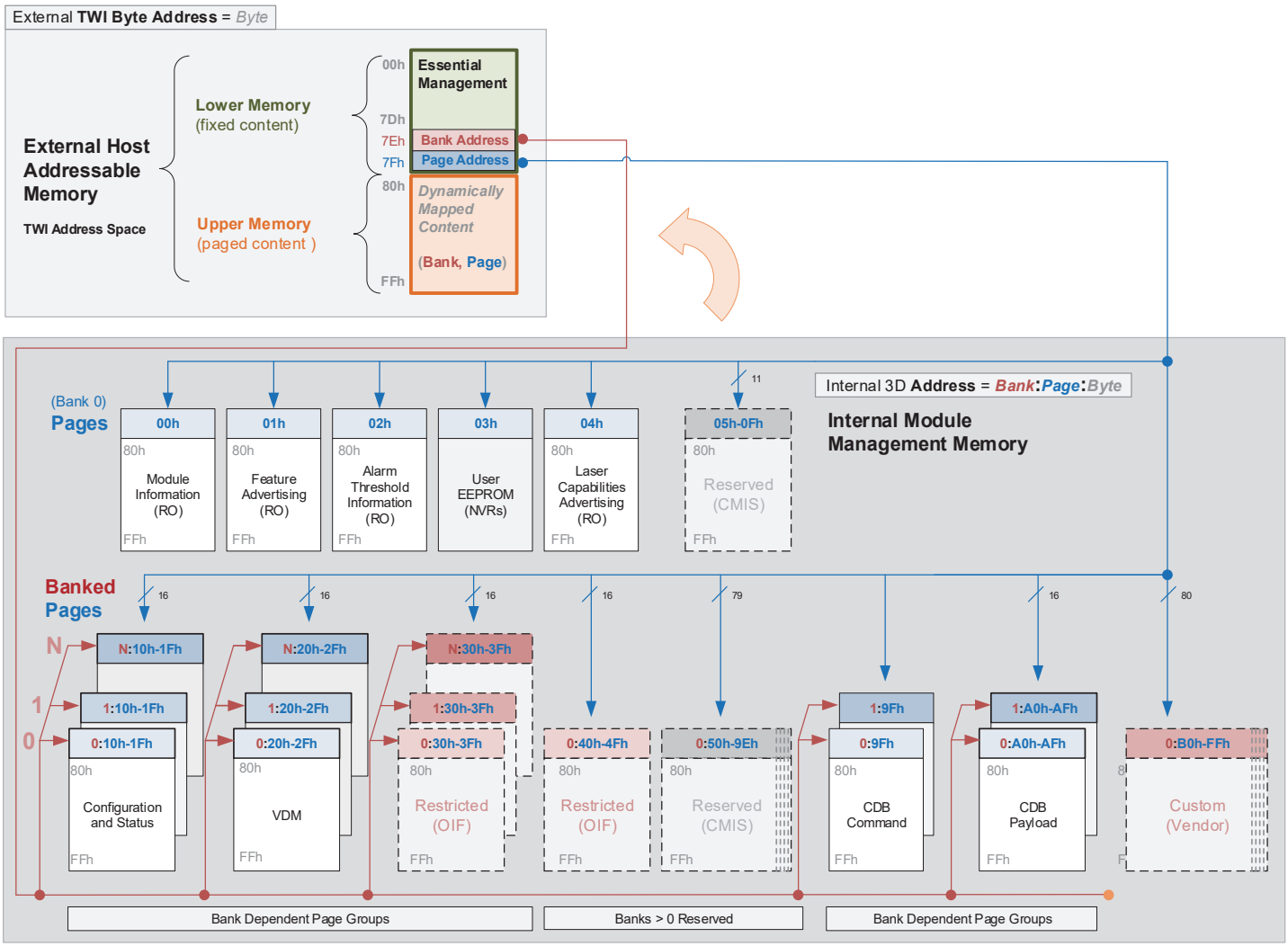


PCB Viewed From Bottom



Digital Diagnostic Memory Map

Digital Diagnostics Monitoring is available on all QSFP-DD products. A two-wire serial interface provides users access to the module with a high clock frequency up to 100 KHz. The control interface and memory map of the QSFP-DD modules are compliant with CMIS (Common Management Interface Specification) for pluggable transceivers. The memory space is arranged into a lower 128 bytes page and multiple upper space pages.



EEPROM Serial ID Memory Contents

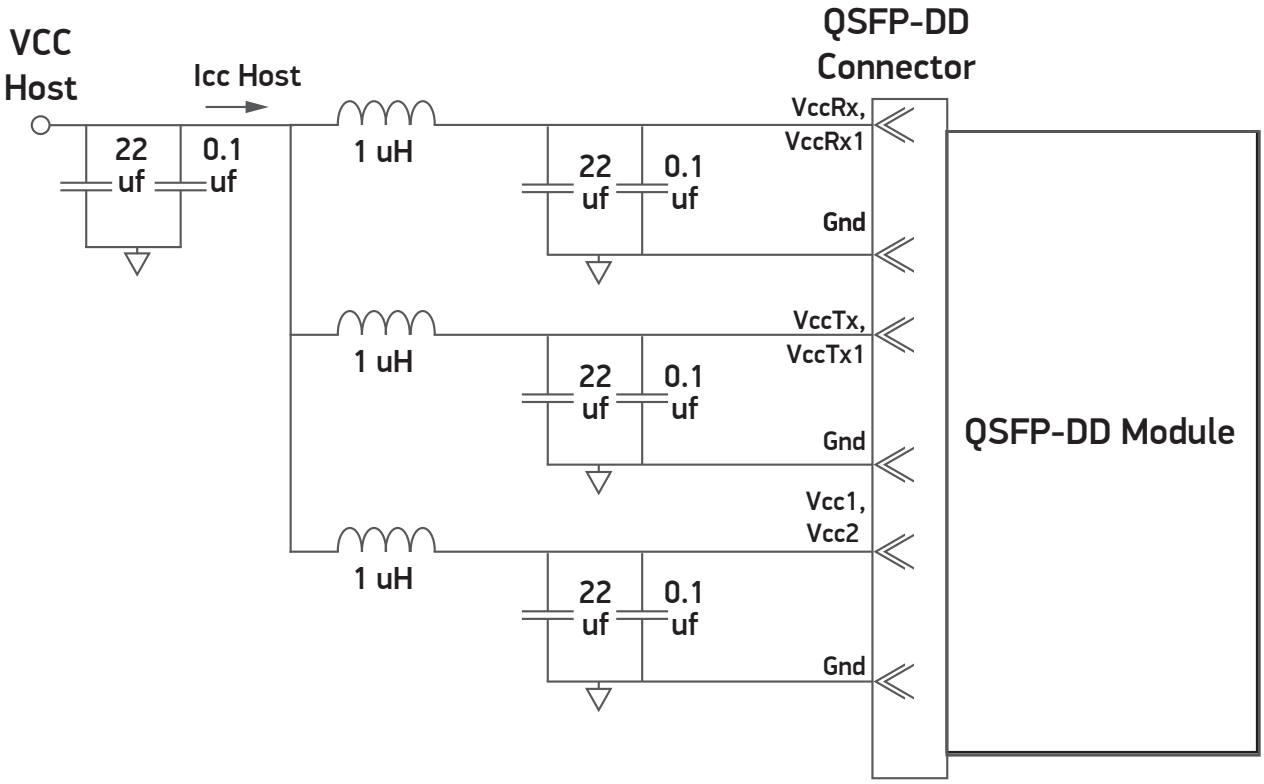
CMIS transceivers define the lower 128 bytes of the two-wire serial bus address space for access to a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent accesses. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed. The lower page is subdivided into several areas as illustrated.

Address	Size	Subject Area	Description
0-2	3	Management Characteristics	Basic information about how this module is managed
3	1	Global Status Information	Current state of module, interrupt signal status
4-7	4	Flags Summary	Summary of flags set on specific pages (and banks)
8-13	6	Module-Level Flags	Flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command
39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering module fault state
42-63	22	-	Reserved[22]
64-84	21	-	Custom[21]
85-117	33	Supported Applications Advertising	Applications supported by module data path(s)
118-125	8	Password Facilities	Password entry and change (mechanism only)
126-127	2	Page Mapping	Page mapping into host addressable upper memory

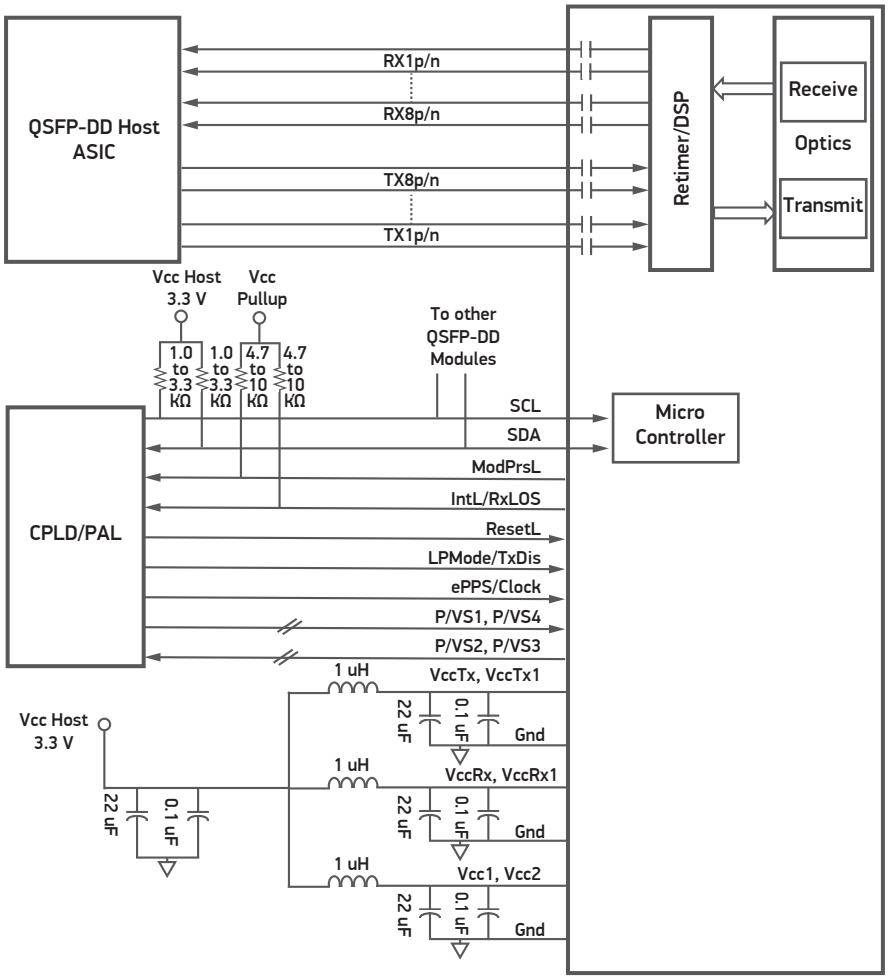
Data Address	Name of Field	Contents (Hex)	Description
128	Identifier	18	QSFP-DD
129-144	Vendor Name	45 64 67 65 63 6F 72 65 20 20 20 20 20 20 20 20	Edgecore (ASCII)
145-147	Vendor OUI	5A ED 67	-
148-163	Vendor PN	45 54 38 30 30 32 2D 53 52 38 20 20 20 20 20 20	“ET8002-SR8” (ASCII)
164-165	Vendor REV	31 30	1.0 (ASCII)
166-181	Vendor SN	32 33 32 38 31 30 30 30 30 31 20 20 20 20 20 20	“2328100001”
182-189	Date Code	32 33 30 31 31 36 20 20	Year (2 bytes), Month (2 bytes), Day (2 bytes) “230616”
190-199	CLEI Code		-
200-201	Module Power Characteristics	C0 40	Power class 7, 16 W Maximum
202	Cable Assembly Link Length	00	
203	Connector Type	28	MPO 1x16
204-209	Copper Cable Attenuation	00 00 00 00 00 00	-
210	Media Lane Information	00	
211	Cable Assembly Information	00	
212	Media Interface Technology	00	850 nm VCSEL
213-220	Reserved	00	
221	Custom	00	
222	Checksum	xx	
223-255	Custom Info NV	00	

Note:
1. The “xx” byte should be filled in according to practical case. For more information, please refer to the related document of CMIS transceivers.

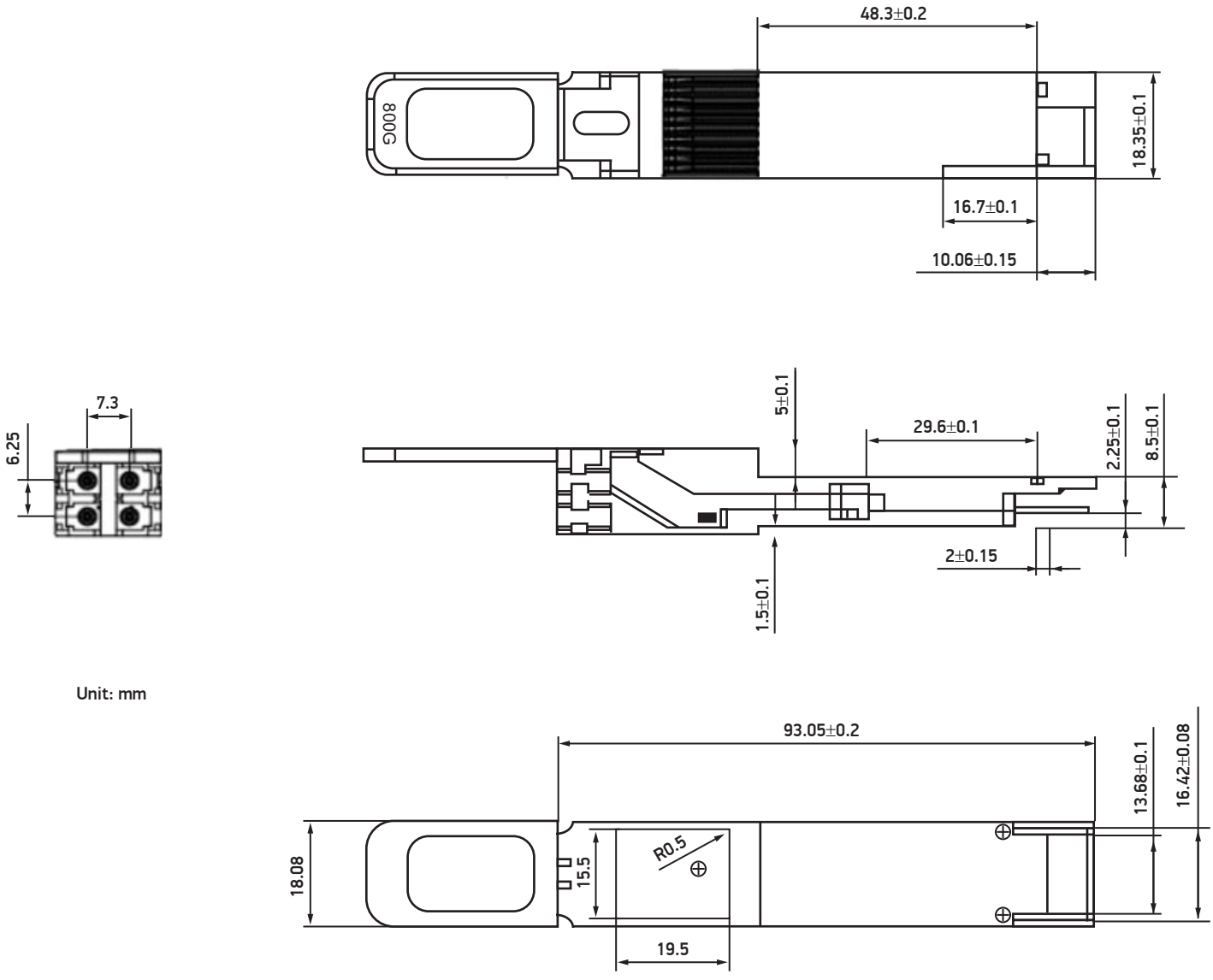
Recommended Host Board Power Supply Filter Network



Recommended Application Interface Block Diagram



Mechanical Specifications



Unit: mm

Warranty

Please check www.edge-core.com for the warranty terms in your country.

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