

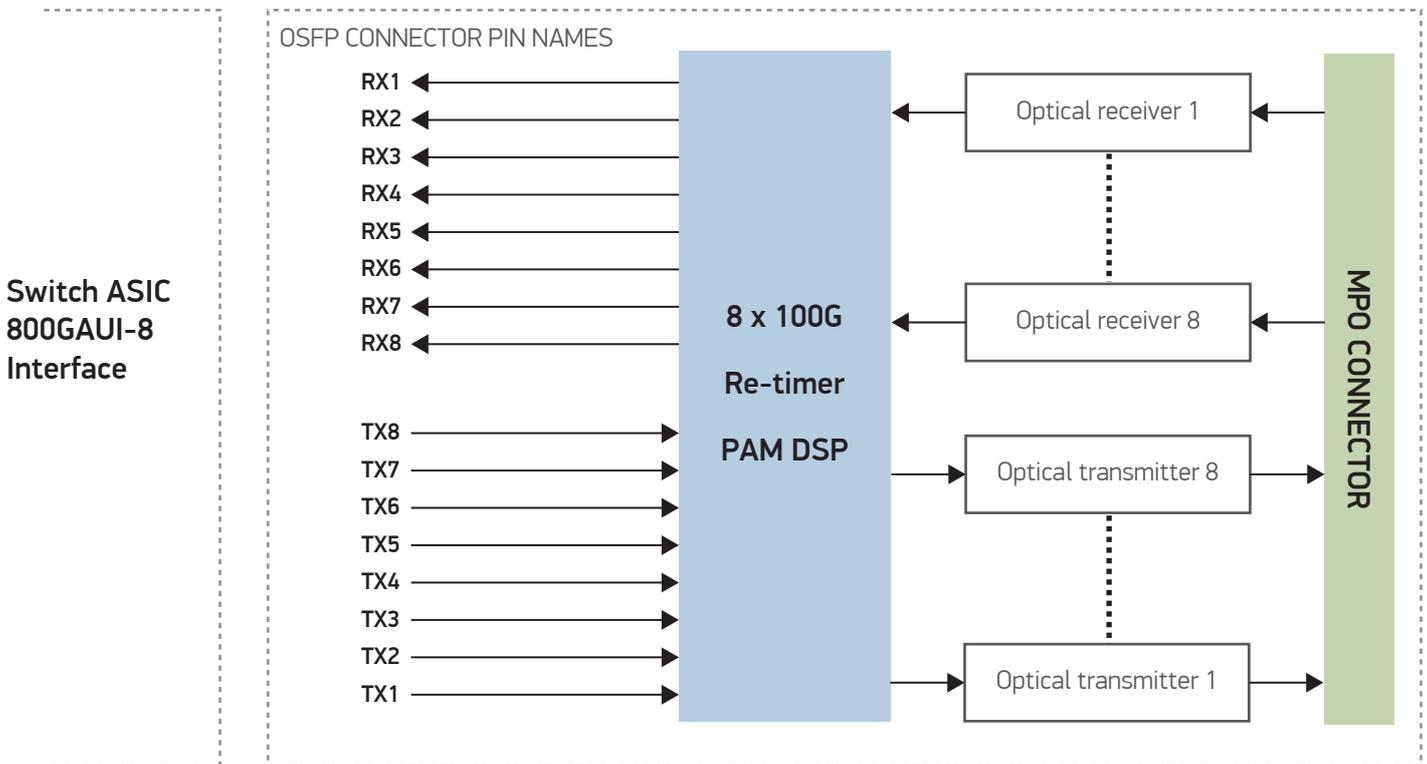
800G QSFP-DD-2xDR4 500m Transceiver

ET8002-2DR4



Based on a 5nm DSP and cooled 1310 EML laser technology, the ET8002-2DR4 is a QSFP-DD 2 x 400G-DR4 transceiver module, compliant with the 800 Gigabit hot-pluggable QSFP-DD Multi-Source Agreement (MSA) used for up to 8 x 100G PAM4 data rates over 500m of single mode fiber.

Optical PMD Illustration



Product Features

- Hot-pluggable QSFP112-DD form factor
- Compliant with IEEE Std 802.3cu 400GBASE-DR4
- Compliant to QSFP-DD MSA
- 8 x 100G PAM4/8 x 50G PAM4 data rates
- Electrical interface compliant with 100Gbps per lane defined by IEEE 802.3ck
- Dual APC MPO-12 receptacles
- Cooled 1310 EML laser
- 5nm DSP for low power dissipation: <14 W
- I²C management interface compliant to CMIS Rev5.0 with integrated Digital Diagnostics Monitoring
- Up to 500 m on 9/125um SMF
- Single 3.3 V power supply
- Class 1 laser safety certified
- Operating case temperature range: 0°C to 70 °C
- RoHS6 compliant

Applications

- High-speed Ethernet networks
- 2 x 400G-DR4 applications

Ordering Information

Model Name	Transmitter	Output Power OMA ¹ @106.25G	Receiver	OMA Sensitivity ² @106.25G	Reach	Case Temp.	DDMI	CMIS
ET8002-2DR4	Cooled EML	-0.8 ~ +4.2dBm	PIN	<-3.9dBm	500m	0~70°C	Yes	CMIS5.0

Notes:

1. Refer to Transmitter Optical Characteristics details.
2. Refer to Receiver Optical Characteristics details

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	°C
Relative Humidity	RH	15	85	%
Supply Voltage	V_{CC}	-0.5	3.6	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_C	0	25	70	°C
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Data Rate per Channel		-	53.125±100ppm	-	GBd
Modulation Format			PAM4		

Transceiver Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Power Dissipation	P_D	-	-	14	W	
Input Differential Impedance	Z_{IN}	90	100	110	Ω	-
Differential Data Input Swing	$V_{IN,P-P}$	180	-	900	mVP-P	-

Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Output Differential Impedance	Z_O	90	100	110	Ω	
Differential Data Output Swing	$V_{OUT,P-P}$	300	-	850	mVP-P	1

Notes:

1. Internally AC coupled, but requires an external 100 Ω differential load termination.

Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Lane Wavelengths	λ	1304.5	1311	1317.5	nm	1
Side-mode Suppression Ratio	SMSR	30	-	-	dB	2
Average Launch Power, each lane	P_{avg}	-2.9	-	4	dBm	3
Outer Optical Modulation Amplitude, each lane	OMA_{outer}	-0.8	-	4.2	dBm	3
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ			3.4	dB	4
Launch Power in OMA_{outer} Minus TDECQ, each lane	$OMA-TDECQ$	-2.2			dBm	
Extinction Ratio	ER	3.5	-	-	dB	-
Average Launch Power of OFF Transmitter	P_{off}			-15	dBm	
Optical Return Loss Tolerance	ORLT			21.4	dB	
Transmitter Reflectance				-26	dB	

Note:

1. 13nm width.
2. Modulated.
3. Class 1 laser safety per FDA/CDRH and EN (IEC) 60825 regulations.
4. 53.125GBd PAM4.

Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Lane Wavelengths	λ	1304.5	1311	1317.5	nm	1
Receiver Sensitivity, each lane (OMA_{outer})				-3.9	dBm	2
Receiver Overload, each lane (P_{avg})	P_{OL}	4		-	dBm	3
Damage Threshold, each lane		5		-	dBm	
Receive Power, each lane (OMA_{outer})	OMA	-		4.2	dBm	
Receiver Reflectance				-26	dB	
LOS De-Assert	LOSD			-10	dBm	4
LOS Assert	LOSA	-16			dBm	4
LOS Hysteresis		0.5			dBm	

Notes:

1. 13nm width.
2. 53.125GBd@BER<2.4x10⁻⁴ and PRBS²³¹-1, per channel.
3. Per channel.
4. Average power.

Electrical Pin Description

Pin	Name	Function/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3 V Power Supply Receiver	2
11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL/RxLOS	Interrupt/Optional RxLOS	
29	VccTx	3.3 V Power Supply Transmitter	2
30	Vcc1	3.3 V Power Supply	2
31	LPMoDe/TxDis	Low Power Mode/Optional TX Disable	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	

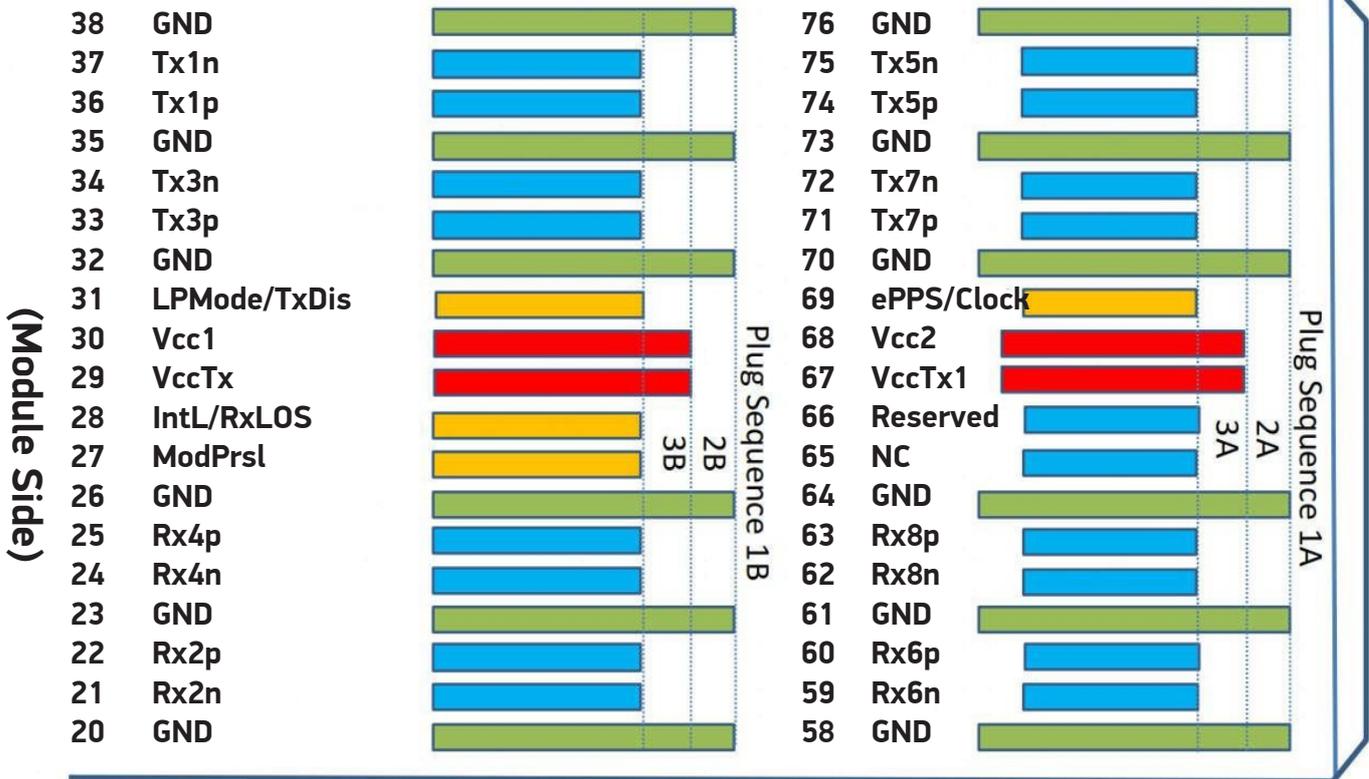
Electrical Pin Description

Pin	Name	Function/Description	Notes
44	Tx8p	Transmitter Non-Inverted Data Input	
45	GND	Ground	1
46	P/VS4	Programmable/Module Vendor Specific 4	4
47	P/VS1	Programmable/Module Vendor Specific 1	4
48	VccRx1	3.3 V Power Supply	2
49	P/VS2	Programmable/Module Vendor Specific 2	4
50	P/VS3	Programmable/Module Vendor Specific 3	4
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3 V Power Supply	2
68	Vcc2	3.3 V Power Supply	2
69	ePPS/Clock	1PPS PTP Clock or Reference Clock Input	5
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	1

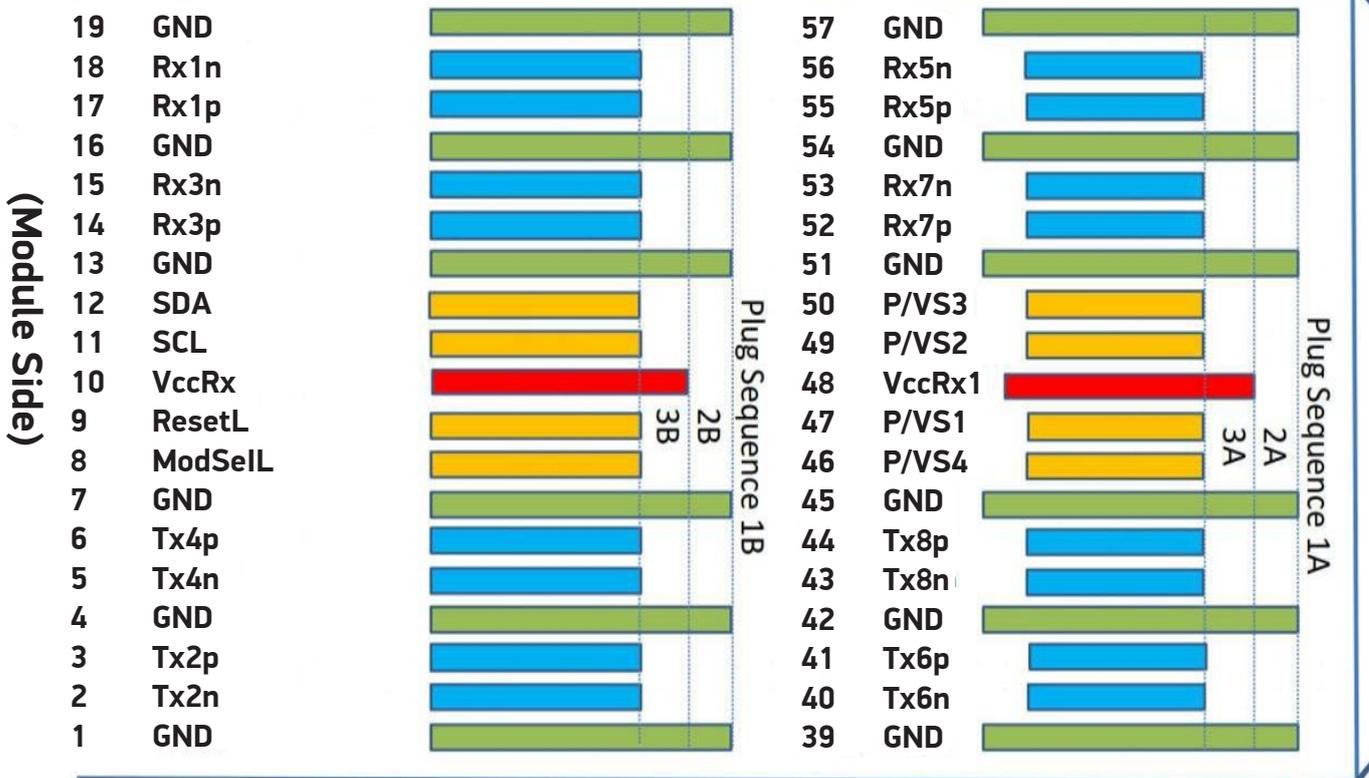
Note:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal- common ground plane. Each connector GND contact is rated for a steady state current of 500mA.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500mA.
3. Reserved pad recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 kΩ to ground on the host.
4. Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.
5. For host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module.

PCB Viewed From Top

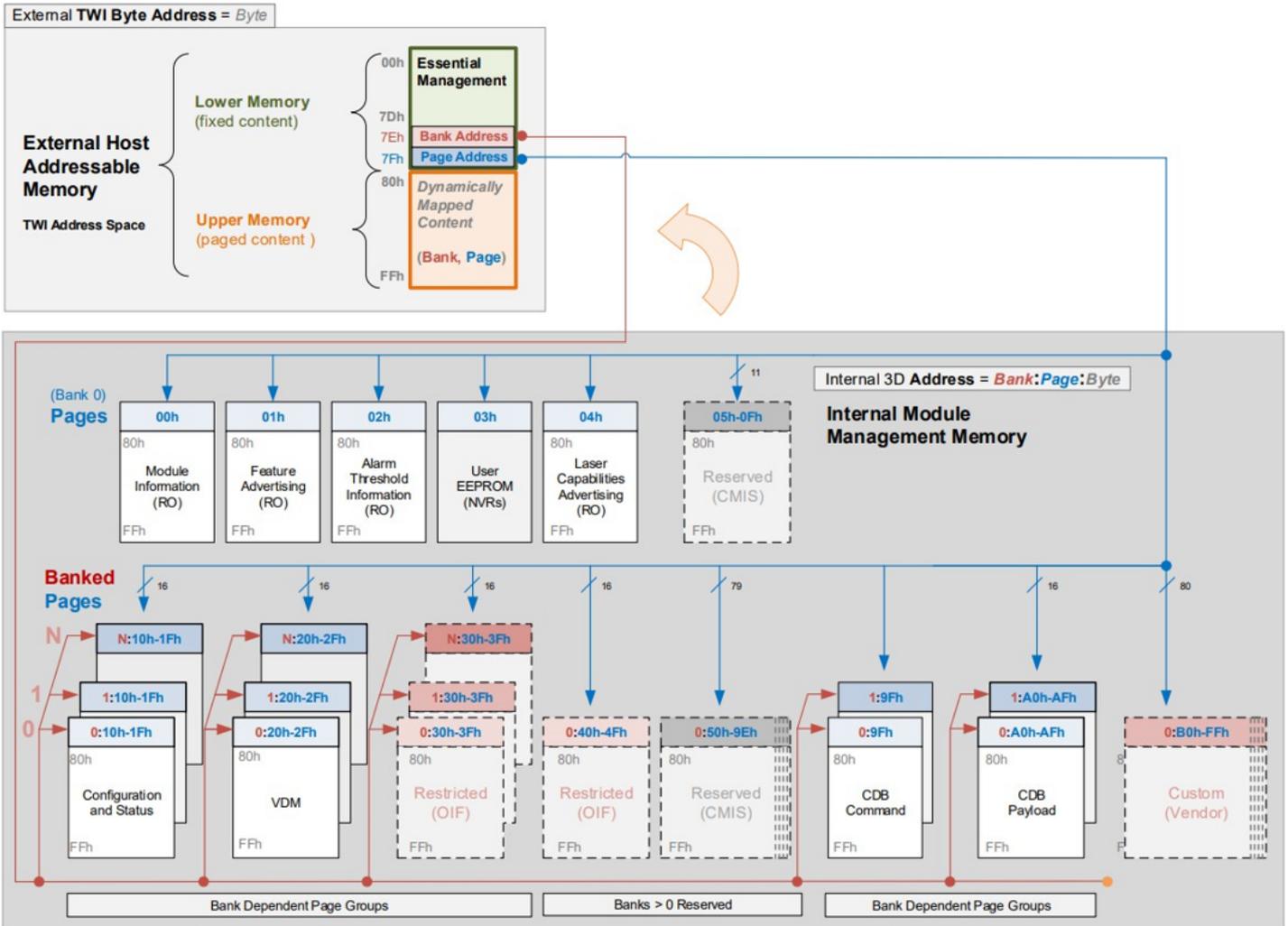


PCB Viewed From Bottom



Digital Diagnostic Memory Map

Digital Diagnostics Monitoring is available on all OSFP products. A 2-wire serial interface provides access to the module with a high clock frequency up to 100 KHz. The control interface and memory map of the OSFP modules are compliant with CMIS (Common Management Interface Specification) for pluggable transceivers. The memory space is arranged into a lower 128 bytes page and multiple upper space pages.



EEPROM Serial ID Memory Contents

CMIS transceivers define the lower 128 bytes of the two-wire serial bus address space for access to a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent accesses. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed. The lower page is subdivided into several areas as illustrated.

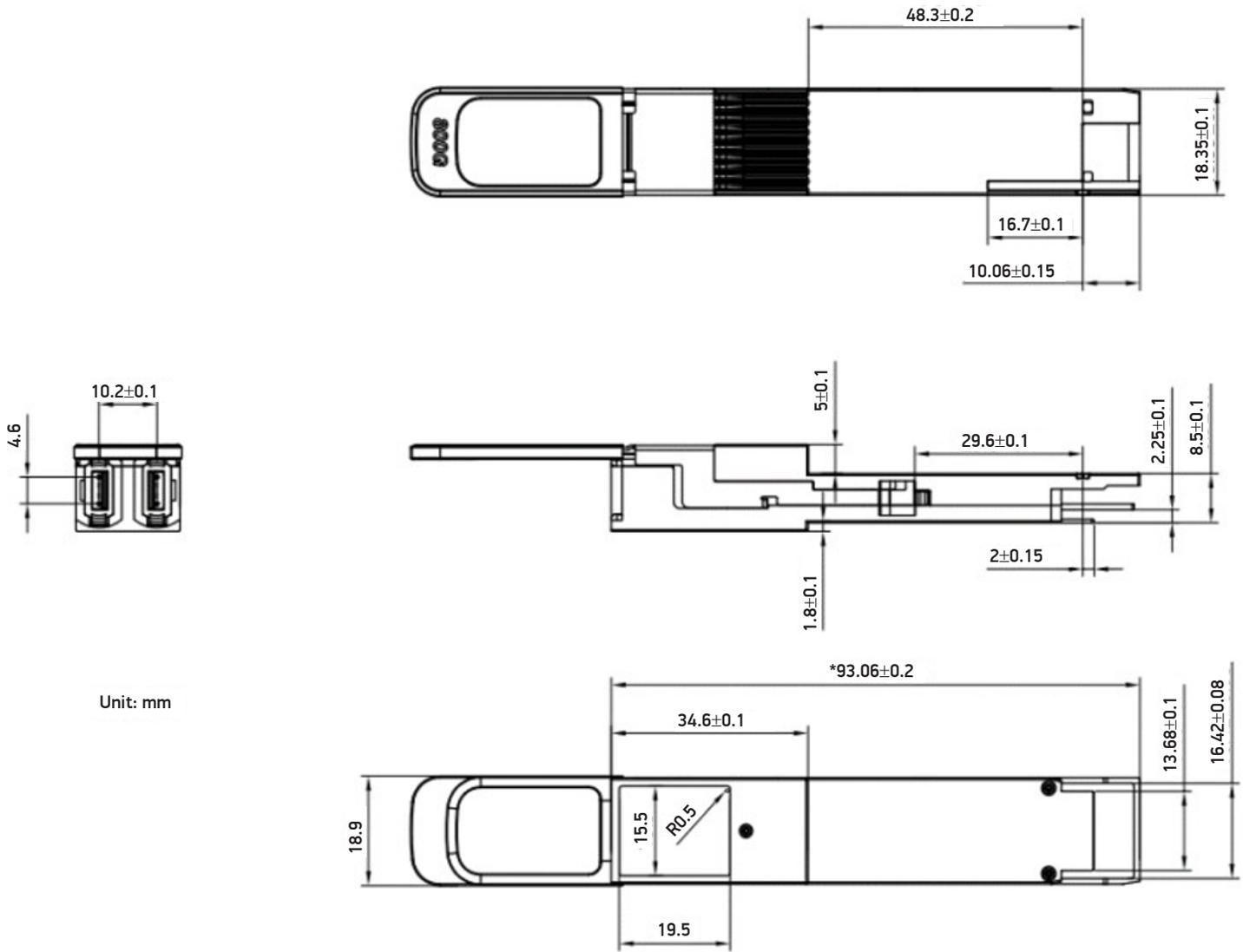
Address	Size	Subject Area	Description
0-2	3	Management Characteristics	Basic information about how this module is managed
3	1	Global Status Information	Current state of module, interrupt signal status
4-7	4	Flags Summary	Summary of flags set on specific pages (and banks)
8-13	6	Module-Level Flags	Flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command
39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering module fault state
42-63	22	-	Reserved[22]
64-84	21	-	Custom[21]
85-117	33	Supported Applications Advertising	Applications supported by module data path(s)
118-125	8	Password Facilities	Password entry and change (mechanism only)
126-127	2	Page Mapping	Page mapping into host addressable upper memory

Data Address	Name of Field	Contents (Hex)	Description
128	Identifier	18	QSFP-DD
		45 64 67 65	
129-144	Vendor Name	63 6F 72 65	Edgecore (ASCII)
		20 20 20 20	
		20 20 20 20	
145-147	Vendor OUI	5A ED 67	-
		45 54 38 30	
148-163	Vendor PN	30 32 2D 32	"ET8002-2DR4" (ASCII)
		44 52 34 20	
		20 20 20 20	
164-165	Vendor REV	31 30	1.0 (ASCII)
		32 33 32 38	
166-181	Vendor SN	31 30 30 30	"2328100001"
		30 31 20 20	
		20 20 20 20	
182-189	Date Code	32 33 30 31	Year (2 bytes), Month (2 bytes), Day (2 bytes)
		31 36 20 20	"230616"
190-199	CLEI Code		-
200-201	Module Power Characteristics	C0 38	Power class 7, 14W Maximum
202	Cable Assembly Link Length	00	
203	Connector Type	0C	MPO 1x12
204-209	Copper Cable Attenuation	00 00 00 00	-
		00 00	
210	Media Lane Information	00	
211	Cable Assembly Information	00	
212	Media Interface Technology	06	1310nm EML
213-220	Reserved	00	
221	Custom	00	
222	Checksum	xx	
223-255	Custom Info NV	00	

Note:

1. The "xx" byte should be filled in according to practical case. For more information, please refer to the related document of CMIS transceivers.

Mechanical Specifications



Unit: mm

Warranty

Please check www.edge-core.com for the warranty terms in your country.

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