1–3m, 800 Gbps OSFP to 2 x 400G QSFP112 Breakout Cable

ET8001B2D-xM-Q

The ET8001B2D-xM-Q is a 1–3 m short passive fan-out copper direct attach cable (DAC) featuring one 800G OSFP connector and two 400G QSFP112 connectors. The OSFP DAC breakout solution enables hardware manufacturers to achieve high port density, flexible configuration, and efficient utilization while maintaining low cost and reduced power consumption. These high-speed cable assemblies are designed to meet and exceed IEEE Ethernet industry-standard requirements for performance and reliability, making them ideal for 800G to 2 × 400G breakout applications in next-generation data center and AI infrastructure deployments.

Key Features and Benefits

- OSFP module compliant with OSFP MSA
- QSFP112 modules compliant with QSFP112 MSA
- Supports 112G PAM4 signaling per lane
- Enables 800 Gbps to 2 × 400 Gbps breakout transmission
- Passive copper DAC solution with link length up to 3 m
- Designed for high port density, flexible configuration, and low power consumption
- Built-in EEPROM functions for module identification and management
- Operating case temperature: 0°C to +70°C
- RoHS 2.0 compliant

Applications

- 800G to 2 × 400G breakout cabling in data center environments
- High-density switch-to-switch or switch-to-server interconnections
- AI/ML and HPC clusters requiring high-bandwidth scale-out connectivity
- Spine–leaf and fabric architectures using ultra-high-bandwidth switches and routers
- Data center cabling infrastructure for next-generation Ethernet deployments

Recommended Operating Conditions

Parameter	Symbol	Min.	Max	Unit
Storage Temperature	Tst	0	80	℃
Case Operating Temperature	Topc	0	70	℃
Supply Voltage	Vcc3	3.14	3.47	V
Relative Humidity	RH	5	80	%

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.
Storage Temperature	TS	-40	85	℃
Relative Humidity	RH	5	95	%
Supply Voltage	Vcc	-0.5	3.6	V

Pin Map (OSFP Side)

60	GND			GND	1
59	Tx1p			Tx2p	2
58	Tx1n			Tx2n	3
57	GND			GND	4
56	Tx3p			Tx4p	5
55	Tx3n			Tx4n	6
54	GND			GND	7
53	Tx5p			Tx6p	8
52	Tx5n			Tx6n	9
51	GND			GND	10
50	Tx7p			Tx8p	11
49	Tx7n			Tx8n	12
48	GND			GND	13
47	SDA			SCL	14
46	VCC			VCC	15
45	VCC			VCC	16
44	INT/RSTn			LPWn/PRSn	17
43	GND			GND	18
42	Rx8n			Rx7n	19
41	Rx8p			Rx7p	20
40	GND			GND	21
39	Rx6n			Rx5n	22
38	Rx6p			Rx5p	23
37	GND			GND	24
36	Rx4n			Rx3n	25
35	Rx4p			Rx3p	26
34	GND			GND	27
33	Rx2n			Rx1n	28
32	Rx2p			Rx1p	29
31	GND			GND	30

Module Card Edge

Pin Description (OSFP Side)

Pad	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	TransmitterData Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial Interface Clock	LVCMOS-I/O	BI-directional	3	1
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low Power Mode/Module Present	Multi-Level	BI-directional	3	2
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	

Pin Description (OSFP Side)

Pad	Symbol	Description	Logic	Direction	Plug Sequence	Notes
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level	Bi-directional	3	2
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial Interface Data	LVCMOS-I/O	Bi-directional	3	1
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Notes:

1. Open-Drain with pull-up resistor on host.
2. See pin description of OSFP MSA for required circuit.

Pin Map (QSFP Side)

38	GND			GND	1
37	TX1n			TX2n	2
36	TX1p			TX2p	3
35	GND			GND	4
34	TX3n			TX4n	5
33	TX3p			TX4p	6
32	GND			GND	7
31	LPMode/TxDis			ModSelL	8
30	Vcc1			ResetL	9
29	VccTx			VccRx	10
28	IntL/RxLOSL			SCL	11
27	ModPrsL			SDA	12
26	GND			GND	13
25	RX4p			RX3p	14
24	RX4n			RX3n	15
23	GND			GND	16
22	RX2p			RX1p	17
21	Rx2n			RX1n	18
20	GND			GND	19

Module Card Edge

Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin Description (QSFP Side)

Pad	Symbol	Description	Plug Sequence	Notes
1	GND	Transmitter Ground (Common with Receiver Ground)	1	1
2	TX2n	Transmitter Inverted Data Input	3	
3	TX2p	Transmitter Non-Inverted Data Input	3	
4	GND	Transmitter Ground (Common with Receiver Ground)	1	1
5	TX4n	Transmitter Inverted Data Input	3	
6	TX4p	Transmitter Non-Inverted Data Input	3	
7	GND	Transmitter Ground (Common with Receiver Ground)	1	1
8	ModeSelL	Module Select	3	
9	ResetL	Module Reset	3	
10	VccRx	+3.3 V Power Supply Receiver	2	3
11	SCL	2-wire Serial Interface Clock	3	
12	SDA	2-wire Serial Interface Data	3	
13	GND	Transmitter Ground (Common with Receiver Ground)	1	1
14	RX3p	Receiver Non-Inverted Data Output	3	
15	RX3n	Receiver Inverted Data Output	3	
16	GND	Transmitter Ground (Common with Receiver	1	1
17	RX1p	Receiver Non-Inverted Data Output	3	
18	RX1n	Receiver Inverted Data Output	3	
19	GND	Transmitter Ground (Common with Receiver Ground)	1	1
20	GND	Transmitter Ground (Common with Receiver Ground)	1	1
21	RX2n	Receiver Inverted Data Output	3	
22	RX2p	Receiver Non-Inverted Data Output	3	
23	GND	Transmitter Ground (Common with Receiver Ground)	1	1
24	RX4n	Receiver Inverted Data Output	3	
25	RX4p	Receiver Non-Inverted Data Output	3	
26	GND	Transmitter Ground (Common with Receiver Ground)	1	1
27	ModPRsL	Module Present	3	
28	IntL/RxLOS	Interrupt	3	2
29	VccTx	+3.3 V Power Supply Transmitter	2	3
30	Vcc1	+3.3 V Power Supply	2	3
31	LPMode/TxDis	Low Power Mode	3	
32	GND	Transmitter Ground (Common with Receiver Ground)	1	1
33	TX3p	Transmitter Non-Inverted Data Input	3	
34	TX3n	Transmitter Inverted Data Input	3	
35	GND	Transmitter Ground (Common with Receiver Ground)	1	1
36	TX1p	Transmitter Non-Inverted Data Input	3	
37	TX1n	Transmitter Inverted Data Input	3	
38	GND	Transmitter Ground (Common with Receiver Ground)	1	1

Notes:

1. QSFP112 uses common ground (GND) for all signals and supply (power). All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a maximum current of 500 mA.
2. This is an open collector/drain output that on the host board requires a 4.7 kΩ to 10 kΩ pull-up resistor to VccHostUp.
3. VccRx, Vcc1, and VccTx shall be applied concurrently. For power classes 4 and above, the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a maximum current of 1500 mA.

Ordering Information

Model Number	Length	AWG	Region
ET8001B2D-1M-Q	1 M	28	All
ET8001B2D-2M-Q	2 M	26	All
ET8001B2D-3M-Q	3 M	26	All

Warranty
Please check www.edge-core.com for the warranty terms in your country.

For More Information
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