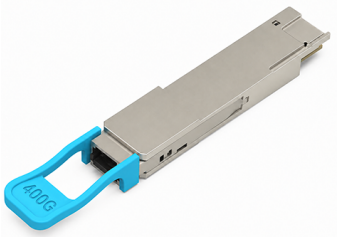
400G 10Km QSFP-DD PLR4 Optical Transceiver

ET7502-PLR4



Edgecore's ET7502-PLR4 transceiver is designed for use in 400 Gbps network applications with a maximum transmission distance of 10 Km. It is a fully integrated optical transceiver modulated using a 4-level pulse amplitude modulation (PAM4) format that transmits and receives optical signals with an aggregated data rate of 425 Gbps over 4 lanes at 1310 nm, each running at 106.25 Gbps. The transceiver is compliant with the QSFP-DD MSA and 100G Lambda MSA optical specifications, and with RoHS.

Product Features

- Compliant with IEEE Std 802.3bs
- Compliant with QSFP-DD MSA
- Compliant with 100G Lambda MSA
- Compliant with CMIS 4.0 management interface specifications
- MPO-12 receptacles
- 1310 nm EML laser
- 8 x 26.5625 GBd PAM4 electrical interface
- Transmission distance up to 10 km SMF
- Single +3.3 V power supply
- Commercial operating temperature: 0℃ to +70℃
- RoHS compliant

Applications

- 400G Ethernet, PLR4, 10 km over parallel SMF
- Data center

Ordering Information

Part Number	Package	Output Power	Receiver	Sensitivity (OMA)	Reach	Case Temp.	DDM	RoHS
ET7502-PLR4	QSFP56-DD	0.3 ~ 4.4 dBm	PIN	< -6.8 dBm	10 km	0~ 70°C	Available	Compliant

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	TS	-40	85	°C
Relative Humidity	RH	0	85	%
Supply Voltage	V_{CC}	-0.5	3.6	V

*Exceeding any one of these values may damage the device permanently

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Case Temperature	Tc	0	25	70	°C
Supply Voltage	Vcc	0	3.3	3.465	V
Data Rate per Channel	-	-	53.125		GBd
Modulation Format			PAM4		

Transceiver Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Note
Module Supply Current	Tc	0	-	2.55	A	-
Power Dissipation	Vcc	0	-	8	W	-
Transmitter	**Symbol**	**Minimum**	**Typical**	**Maximum**	**Unit**	**Note**
Input Differential Impedance	Z_{IN}	-	100	-	Ω	-
Differential Data Input Swing	$V_{IN, P-P}$	180	-	900	mVp-p	-
Receiver	**Symbol**	**Minimum**	**Type**	**Maximum**	**Unit**	
Output Differential Impedance	Zo	-	100	-	Ω	-
Differential Data Output Swing	$V_{OUT, P-P}$	300	-	850	mVp-p	1
Transition Time (20% to 80%)	T_r, T_f	9.5	-	-	Ps	

Notes: 1. Internally AC coupled, but requires an external 100 Ω differential load termination.

Transmitter Optical Characteristics

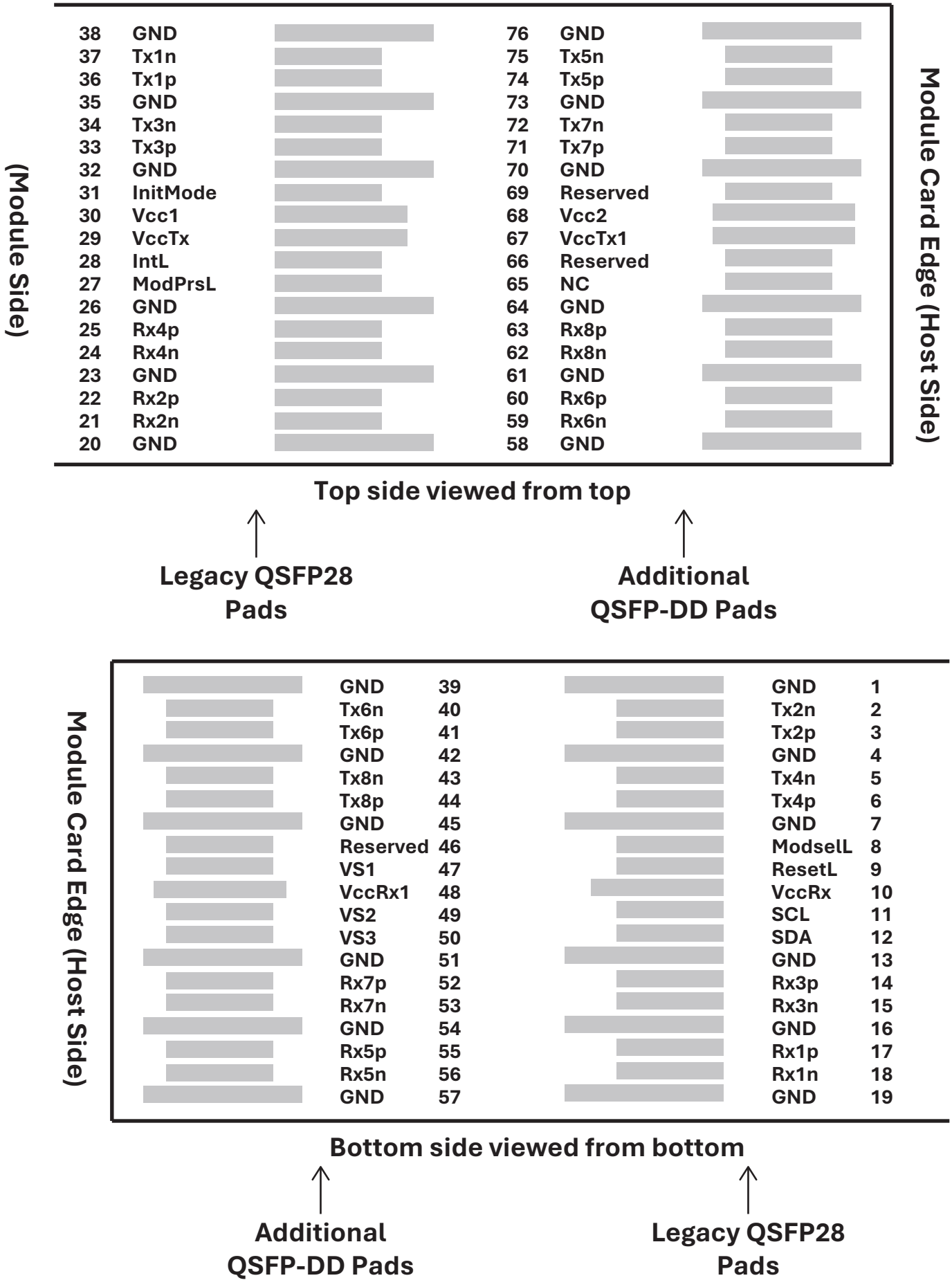
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Note
Lane Wavelengths	λ	1304.5	-	1317.5	nm	
Side-Mode Suppression Ratio	SMSR	30	-	-	dB	-
Average Launch Power, Each Lane	P	-2.7	-	5.1	dBm	-
Outer Optical Modulation Amplitude, Each Lane	OMAouter	0.3	-	4.4	dBm	-
OMAouter Minus TDECQ (min)		-0.6			dBm	
Transmitter and Dispersion Penalty Eye Closure for PAM4, Each Lane	TDECQ	-	-	3.9	dB	-
Extinction Ratio	EX	3.5	-	-	dB	-
Average Launch Power of OFF Transmitter	Poff	-	-	-16	dBm	-
Optical Return Loss Tolerance	ORLT	-	-	15.6	dB	-
Transmitter Reflectance	-	-	-	-26	dB	-

Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Note
Lane Wavelengths	λ	1304.5	-	1317.5	nm	-
Receiver Sensitivity Each Lane (OMAouter) for TECQ<1.4 dB				-6.8	dBm	1
Receiver Sensitivity in Average Power				-6.2	dBm	
Receiver Overload (Pavg)	POL	5.1	-	-	dBm	
Damage Threshold	POL	6.1	-	-	dBm	
Receive Power, Each Lane (OMAouter)	OMA	-	-	4.4	dBm	-
Optical Reflectance	ORL	-	-	-26	dB	-
LOS De-Assert	LOSD	-	-	-12	dBm	-
LOS Assert	LOSA	-18	-	-	dBm	-
LOS Hysteresis	-	0.5	-	-	dB	-

Notes: 1. Measured with PRBS31Q test pattern, 53.125GBd, PAM4, BER<2.4E-4.

Pin Map


(Module Side)
38 GND
37 Tx1n
36 Tx1p
35 GND
34 Tx3n
33 Tx3p
32 GND
31 InitMode
30 Vcc1
29 VccTx
28 IntL
27 ModPrsL
26 GND
25 Rx4p
24 Rx4n
23 GND
22 Rx2p
21 Rx2n
20 GND
76 GND
75 Tx5n
74 Tx5p
73 GND
72 Tx7n
71 Tx7p
70 GND
69 Reserved
68 Vcc2
67 VccTx1
66 Reserved
65 NC
64 GND
63 Rx8p
62 Rx8n
61 GND
60 Rx6p
59 Rx6n
58 GND
Module Card Edge (Host Side)
Top side viewed from top
Legacy QSFP28 Pads
Additional QSFP-DD Pads
Module Card Edge (Host Side)
GND 39
Tx6n 40
Tx6p 41
GND 42
Tx8n 43
Tx8p 44
GND 45
Reserved 46
VS1 47
VccRx1 48
VS2 49
VS3 50
GND 51
Rx7p 52
Rx7n 53
GND 54
Rx5p 55
Rx5n 56
GND 57
GND 1
Tx2n 2
Tx2p 3
GND 4
Tx4n 5
Tx4p 6
GND 7
ModselL 8
ResetL 9
VccRx 10
SCL 11
SDA 12
GND 13
Rx3p 14
Rx3n 15
GND 16
Rx1p 17
Rx1n 18
GND 19
(Module Side)
Bottom side viewed from bottom
Additional QSFP-DD Pads
Legacy QSFP28 Pads

Pin Descriptions

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3 V Power Supply Receiver	2
11	LVCMOS- I/O	SCL	2-wire Serial Interface Clock	
12	LVCMOS- I/O	SDA	2-wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power supply transmitter	2
30		Vcc1	+3.3 V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1

Pin Descriptions

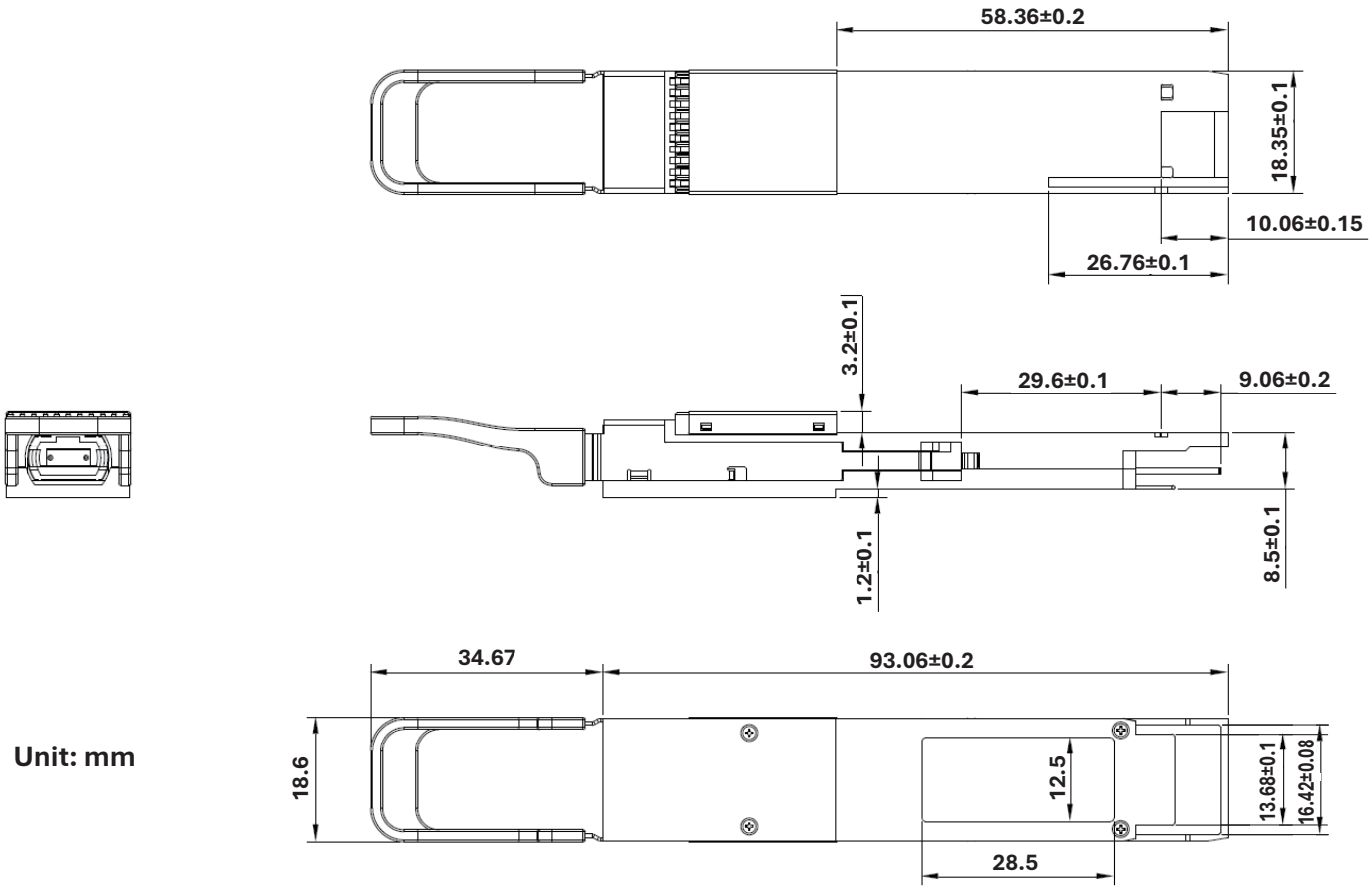
Pin	Logic	Symbol	Description	Notes
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3 V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3 V Power Supply	2
68		Vcc2	3.3 V Power Supply	2
69		Reserved	For Future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

*Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted.
Connect these directly to the host board signal-common ground plane.

*Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the host card edge connector are listed in VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

*Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impedance to GND that is greater than 10 k ohms and less than 100 pF.

Mechanical Specifications



Unit: mm

Warranty

Please check www.edge-core.com for the warranty terms in your country.

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