400G QSFP-DD SR8 Transceiver

ET7502-SR8

Edgecore's QSFP-DD SR8 transceiver module is designed for 400 Gigabit Ethernet links over 100m OM4 multimode fiber. The module has 8 independent electrical input/output channels operating at 53.125 Gbps per channel over 850 nm wavelengths. The electrical interface of the module is compliant with the 400GAUI-8 interface as defined by IEEE 802.3bs, and compliant with QSFP-DD MSA.

Product Features

- Single 3.3 V power supply
- Power dissipation < 10 W
- Up to 100 m over OM4 fiber
- QSFP-DD MSA compliant
- 8x26.5625 GBd (PAM4) electrical interface
- MPO-16 connector (APC)
- Commercial case temperature range of 0°C to 70°C
- VCSEL transmitter
- PIN and TIA array on the receiver side
- I2C Interface with integrated Digital Diagnostic Monitoring
- RoHS compliant (lead-free)

Applications

- 400G-SR8 Ethernet links

Ordering Information

Part Number	Data Rate	Fiber	Distance *(Note 1)	Interface	Temp.	MPO Connector	CMIS
ET7502-SR8	425 Gbps	OM4	100 m	MPO16	0~70°C	APC	CMIS4.0 *(Note1)

Note 1: CMIS4.0 or later versions

Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Signaling Speed per Lane			25.5625±100ppm		GBd
Modulation Format			PAM4		
Center Wavelength	λc	840	850	868	nm
RMS Spectral Width	Δλrms			0.6	nm
Extinction Ratio	ER	3			dB
Transmit OMA Each Lane	TxOMA	-4.5		3	dBm
Transmit Average Each Lane	TxAVG	-6.5		4	dBm
Launch Power in OMA_{outer} minus TDECQ		-5.9			dBm
Transmitter and Dispersion Eye Closure, each Lane	TDECQ			4.5	dB
Average Launch Power of OFF Transmitter, Each Lane				-30	dBm
RIN12OMA				-128	dB/Hz
Optical Return Loss Tolerance				12	dB
Encircled Flux		≥ 86% at 19 um ≤ 30% at 4.5 um			

Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Signaling Speed per Lane			25.5625±100 ppm		
Modulation Format			PAM4		
Center Wavelength	λc	840	850	868	nm
Damage Threshold		5			dBm
Receive Power (OMA) Each Lane	RxOMA			3	dBm
Average Receive Power Each Lane	RxAVG	-8.4		4	dBm
Receiver Reflectance				-12	dB
Stressed Receiver Sensitivity (OMA_{outer})				-3.4	dBm
Receiver Sensitivity (OMA_{outer}), Each Lane	SenOMA			Note 1	dBm
Stressed Eye Closure	SECQ			4.5	dBm
LOS Assert	LOSA	-14			dBm
LOS De-Assert	LOSD			-8	dBm

*Note 1: Sensitivity=max (-6.5, SECQ-7.9) dB with BER<2.4x10-4 pre-FEC.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V

*Exceeding any one of these values may damage the device permanently.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	Tc	0		70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Operating Relative Humidity	RH	5		85	%
Power Dissipation	P_D			10	W

*Power Supply specifications, Instantaneous, sustained and steady state current compliant with QSFP-DD MSA Power Classification.

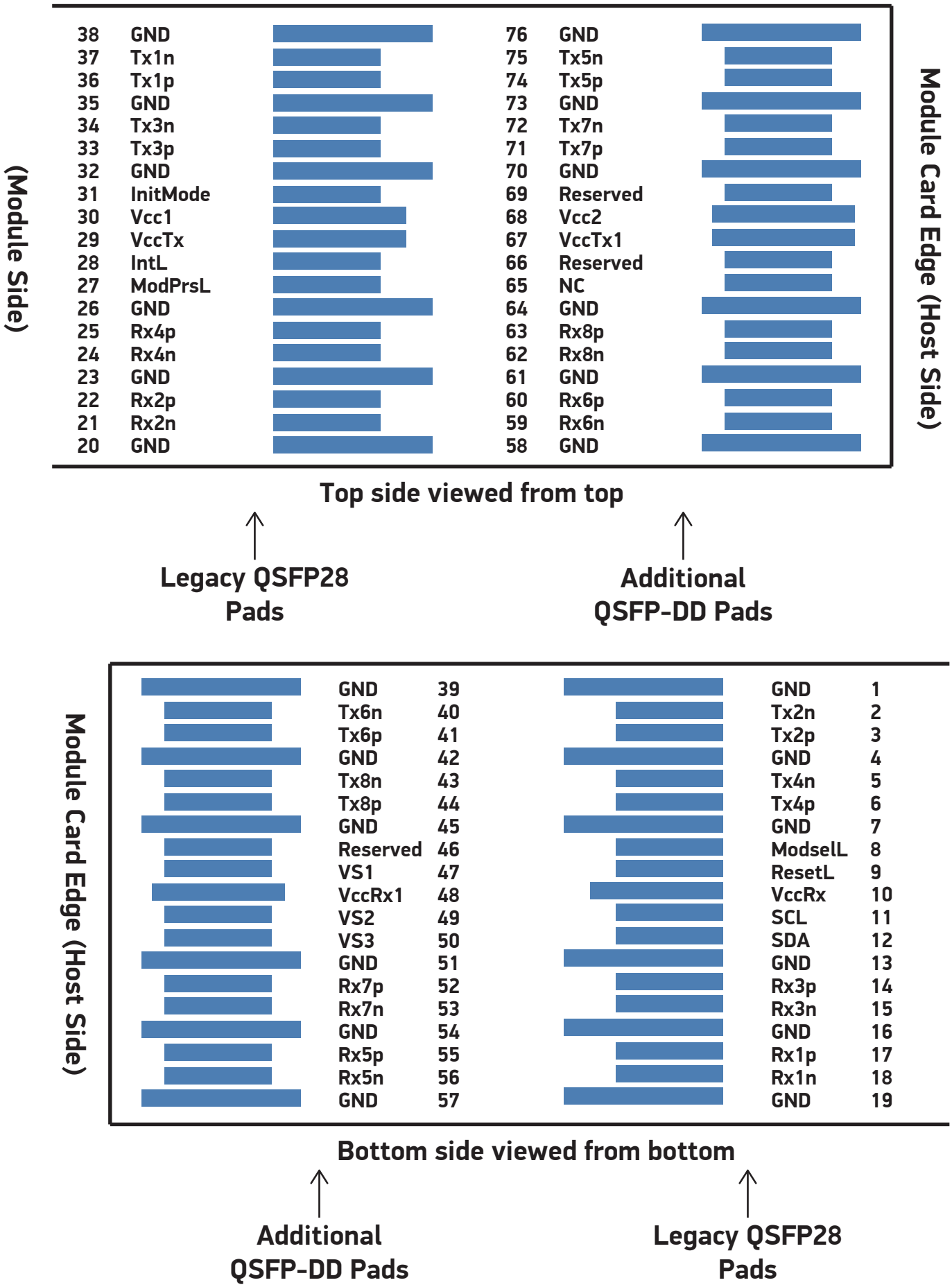
Input Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit	Note
Differential Data Input Swing per Lane	Vin	900			mV_{p-p}	
Differential Input Impedance	Zin	90	100	110	ohm	
AC Common-mode Output Voltage (RMS)				17.5	mV	
Single-ended Voltage		-0.4		3.3	V	
Tolerance Range						
Transition Time (20% to 80%)		10			ps	
DC Common Mode Voltage		-350		2850	mV	

Output Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit	Note
Differential Output Amplitude	Vout			900	mV_{p-p}	
Differential Output Impedance	Zout	90	100	110	ohm	
AC Common-mode Noise (RMS)				17.5	mV	
Near-end ESMW (Eye Symmetry Mack Width)		0.265			UI	
Near-end Eye Height, Differential		70			mV	
Far-end ESMW (Eye Symmetry Mack Width)		0.2			UI	
Far-end Eye Height, Differential		30			mV	
Transition Time (20% to 80%)	tr/t_f	9.5			ps	
DC Common Mode Voltage		-350		2850	mV	

QSFP-DD Transceiver Electrical Pad Layout



Pin Descriptions

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3 V Power Supply Receiver	2
11	LVCMOS- I/O	SCL	2-wire Serial Interface Clock	
12	LVCMOS- I/O	SDA	2-wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power supply transmitter	2
30		Vcc1	+3.3 V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1

Pin Descriptions

Pin	Logic	Symbol	Description	Notes
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3 V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3 V Power Supply	2
68		Vcc2	3.3 V Power Supply	2
69		Reserved	For Future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

*Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted.
Connect these directly to the host board signal-common ground plane.

*Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 Ma.

*Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 Pf.

Warranty

Please check www.edge-core.com for the warranty terms in your country.

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